

# *QIQY6*

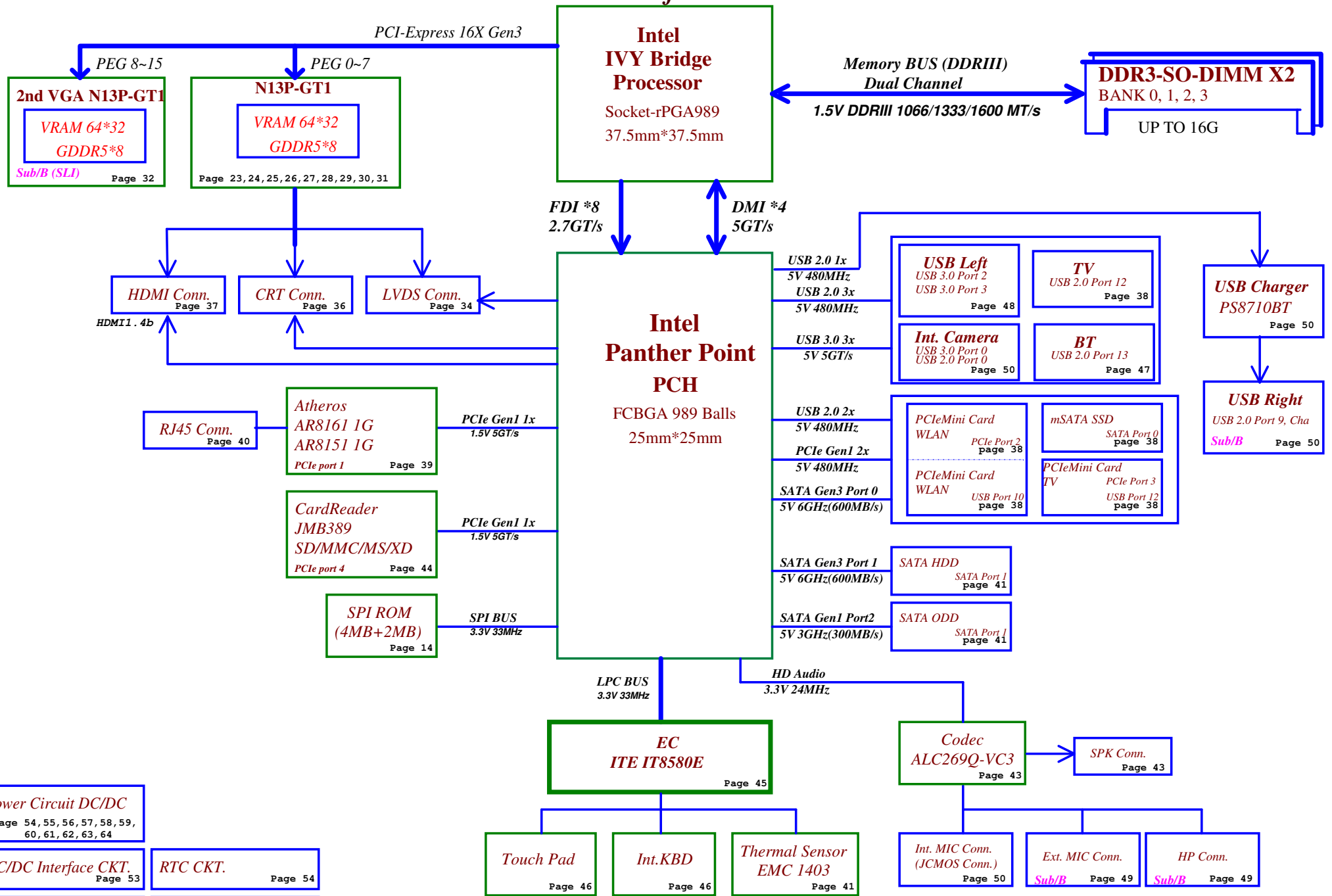
## *Brandy3.0 (Y500)*

### *LA-8692P Rev0.2 Schematic*

*Intel IVY Bridge Processor with DDRIII + Panther Point PCH*  
*nVIDIA N13P GT-1 + 2nd VGA N13P GT-1*  
*2012-02-05 Rev0.2*

Security Classification	LC Future Center Secret Data			Title <b>Cover Page</b>	
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# Chief River



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Voltage Rails				
<div>power plane</div> <div>State</div>	+B	+5VALW  +3VALW	+1.5V	+5VS  +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1	IT8580E	X	X	V	X	X	X	X	X
SMB_EC_DA1	+3VALW			+3VALW					
SMB_EC_CK2	IT8580E	X	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW								+3VS
SMBCLK	PCH	X	X	X	X	V	V	X	X
SMBDATA	+3VALW					+3VS	+3VS		
SML0CLK	PCH	X	X	X	X	X	X	X	X
SML0DATA	+3VALW								
SML1CLK	PCH	V	V	X	V	X	X	V	X
SML1DATA	+3VALW	+3VS	+3VS		+3VS			+3VS	

EC SM Bus1 address EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	Thermal Sensor EMC1403-2	1001_101xb
		Master VGA	0x9E
		Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb



USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
EHCI1	XHCI	0	Camera Camera
		1	
		2	USB Port (Left Side)
		3	USB Port (Left Side)
		4	USB Port (Left Side)
		5	
		6	
		7	
		8	
		9	USB Port (Right Side)
		10	Mini Card(WLAN)
		11	
		12	Mini Card(TV)
EHCI2		13	Blue Tooth

PCIe PORT LIST

Port	Device
1	LAN
2	WLAN
3	TV
4	Card Reader
5	
6	
7	
8	

BOM Structure Table

BOM Structure	BTO Item
HDMI@	HDMI part
TV@	TV module part
CMOS@	CMOS Camera part
8161@	AR8161 LAN part
8151@	AR8151 LAN part
8161S@	AR8161 LAN surge part
8151S@	AR8151 LAN surge part
SURGE@	AR8151&8161 LAN surge part
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
OPT@	For optimus function part
SLI@	For SLI function part
DS3@	Deep S3 support part
GT@	NV chip part
@	Unpop

Hot plug detect for IFP link E

## VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	-	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	-	GPIO16
GPIO17	IN	N/A	GPIO17
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	-	GPIO19

## Performance Mode P0 TDP at Tj = 102 C\* (GDDR5)

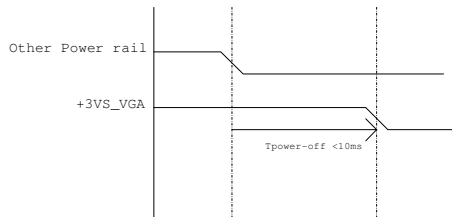
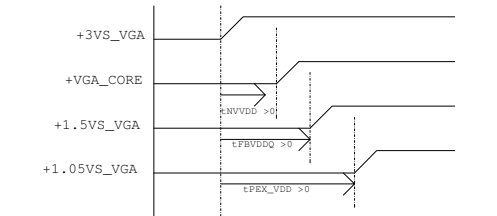
	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
Products	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID		setting	I2C Slave addresses ID
N13P-GT (28nm)	0x0FDB	SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E
			1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GT1 28nm	PU 25K GC6@					PU 5K SLI@	
	PU 10K	PU 5K OPT@, SLI@	PU 45K	PD 5K	PD 10K	PD 5K OPT@	PD 45K

GPU	N13P-GT		
FB Memory (GDDR5)	ROM_SI		
Samsung 2500MHz	K4G10325FD-FC04		
	32Mx32	PD 45K	
Hynix 2500MHz	H5GQ1H24BFR-T2C		
	32Mx32	PD 35K	
Samsung 2500MHz	K4G20325FD-FC04		
	64Mx32	PD 30K	
Hynix 2500MHz	H5GQ2H24AFR-T2C		
	64Mx32	PD 25K	

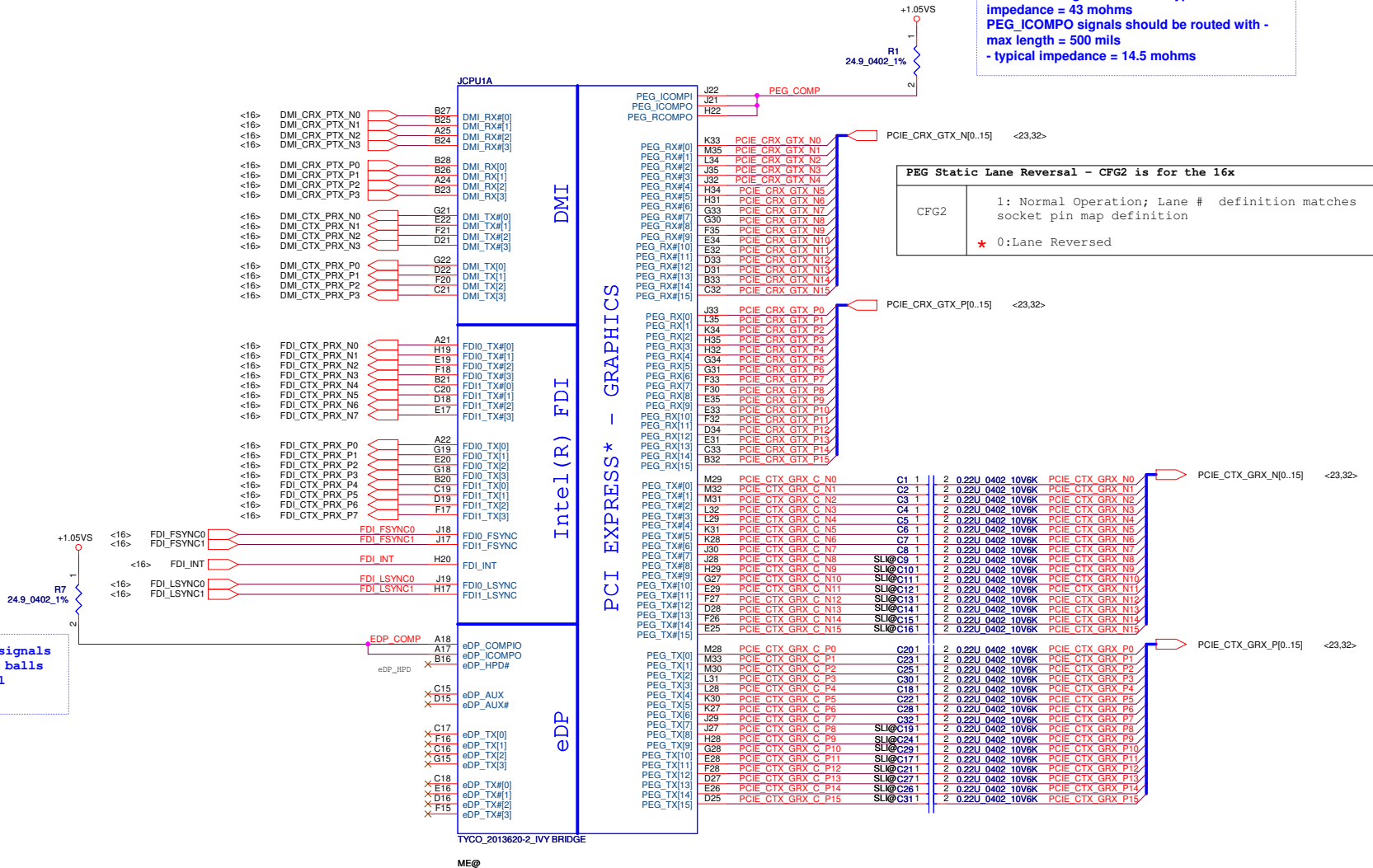


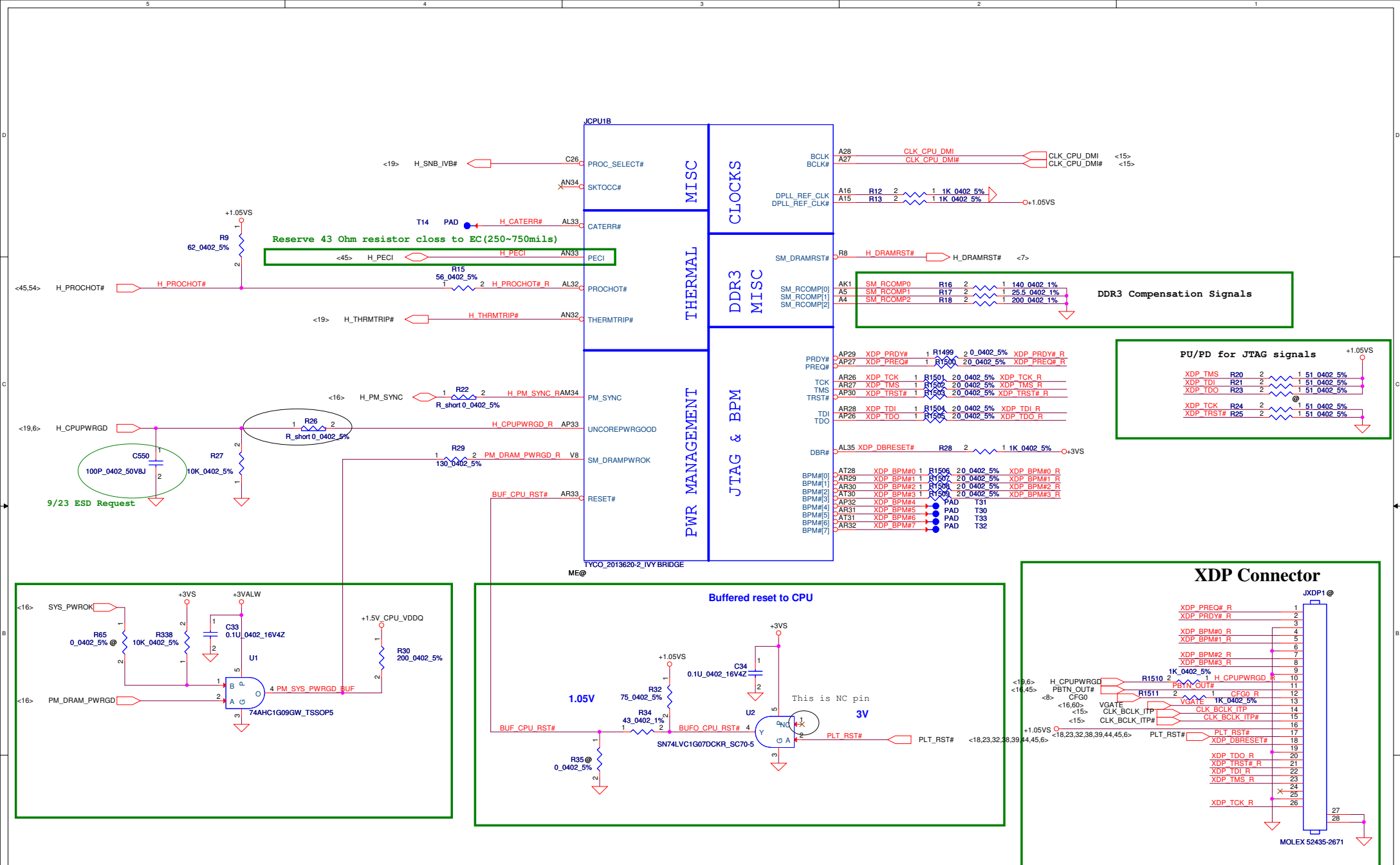
1. all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

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EDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

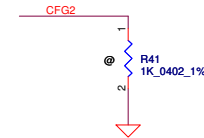
PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



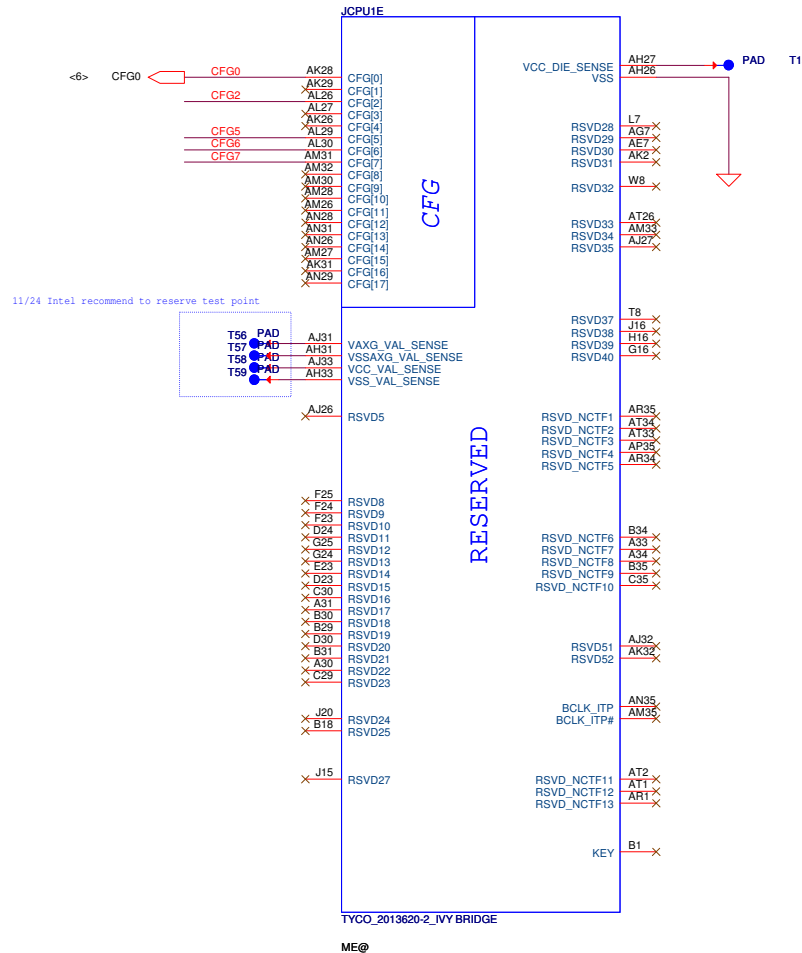




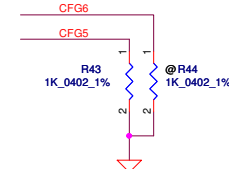
## CFG Straps for Processor



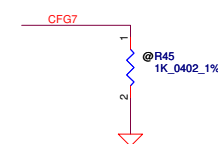
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	<p>★ 1: Normal Operation; Lane # definition matches socket pin map definition</p> <p>0: Lane Reversed</p>



Display Port Presence Strap	
CFG4	<p>★ 1 : Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0 : Enabled; An external Display Port device is connected to the Embedded Display Port</p>



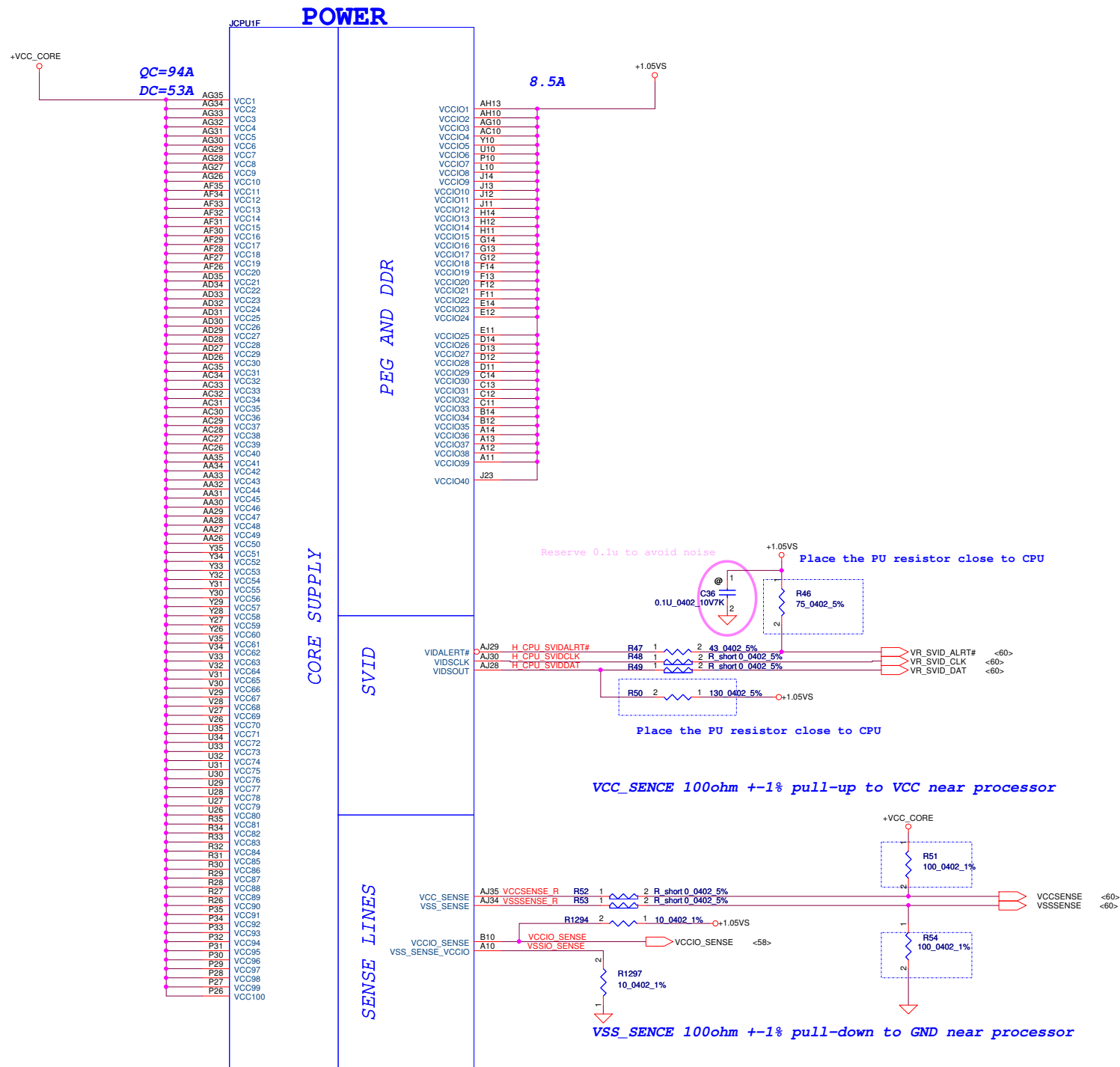
PCIe Port Bifurcation Straps	
CFG[6:5]	<p>11: (Default) x16 - Device 1 functions 1 and 2 disabled</p> <p>★ 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled</p> <p>01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)</p> <p>00: x8,x4,x4 - Device 1 functions 1 and 2 enabled</p>



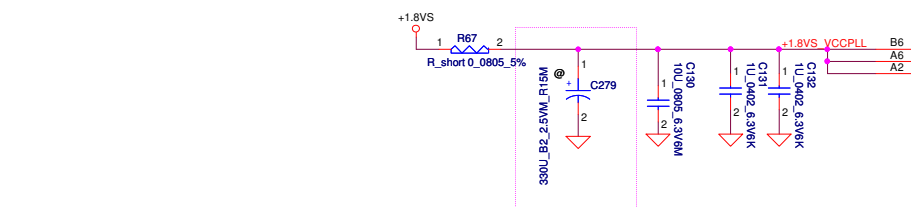
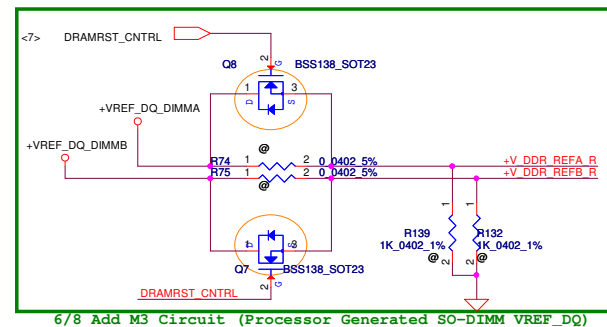
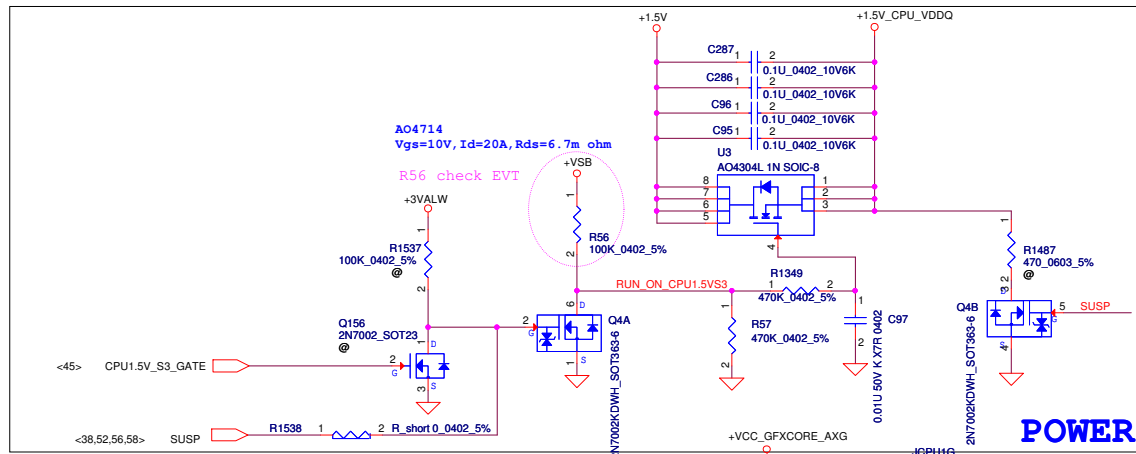
PEG DEFER TRAINING	
CFG7	<p>1: (Default) PEG Train immediately following xxRESETB de assertion</p> <p>0: PEG Wait for BIOS for training</p>

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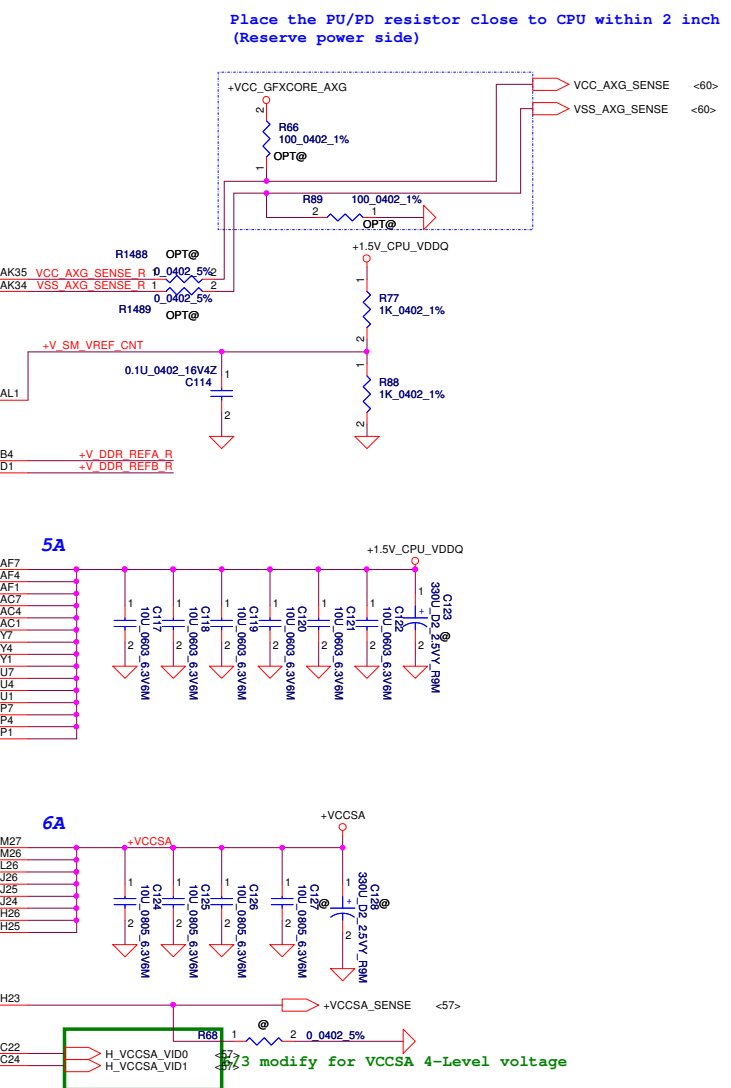


TYCO_2013620-2, MX BRIDGE		LC Future Center Secret Data		Title	
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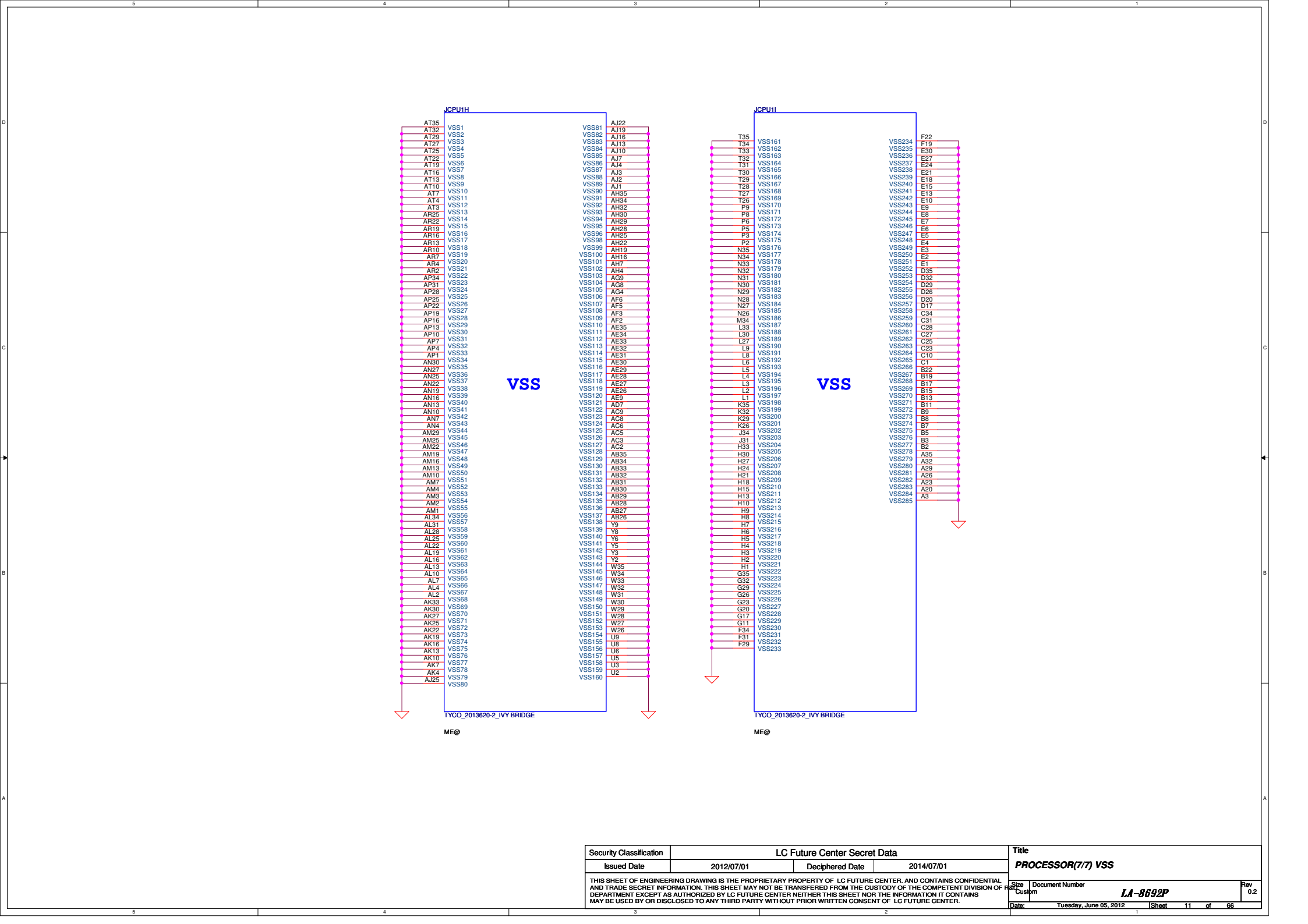


POWER	
46A	AT24 VAXG1
	AT23 VAXG2
	AT20 VAXG3
	AT18 VAXG4
	AT17 VAXG5
	AR24 VAXG6
	AR23 VAXG7
	AR21 VAXG8
	AR20 VAXG9
	AR17 VAXG10
	AP24 VAXG12
	AP23 VAXG13
	AP21 VAXG14
	AP20 VAXG15
	AP18 VAXG16
	AP17 VAXG17
	AN24 VAXG18
	AN23 VAXG19
	AN21 VAXG20
	AN20 VAXG21
	AN18 VAXG22
	AN17 VAXG23
	AM24 VAXG24
	AM23 VAXG25
	AM21 VAXG26
	AM20 VAXG27
	AM18 VAXG28
	AM17 VAXG29
	AL24 VAXG30
	AL23 VAXG31
	AL21 VAXG32
	AL20 VAXG33
	AL18 VAXG34
	AL17 VAXG35
	AK24 VAXG36
	AK23 VAXG37
	AK21 VAXG38
	AK20 VAXG39
	AK18 VAXG40
	AK17 VAXG41
	AJ24 VAXG42
	AJ23 VAXG43
	AJ21 VAXG44
	AJ20 VAXG45
	AJ18 VAXG46
	AJ17 VAXG47
	AH24 VAXG48
	AH23 VAXG49
	AH21 VAXG50
	AH20 VAXG51
	AH18 VAXG52
	AH17 VAXG53
	AH16 VAXG54

SENSE LINES	
VAXG_SENSE	AK35 VCC AXG SENSE R 0.0402 5%
VSSAXG_SENSE	AK34 VSS AXG SENSE R 1 0.0402 5%
SM_VREF	AL1
VREF	B4 +V SM VREF CNT
SA_DIMM_VREFDQ	D1
SB_DIMM_VREFDQ	D1
DDR3 -1.5V RAILS	
VDDQ1	AF7
VDDQ2	AF4
VDDQ3	AF1
VDDQ4	AC7
VDDQ5	AC4
VDDQ6	AC1
VDDQ7	Y7
VDDQ8	Y4
VDDQ9	Y1
VDDQ10	U7
VDDQ11	U4
VDDQ12	U1
VDDQ13	P7
VDDQ14	P4
VDDQ15	P1
SA RAIL	
VCCSA1	M27
VCCSA2	M26
VCCSA3	J26
VCCSA4	J25
VCCSA5	J24
VCCSA6	H26
VCCSA7	H25
VCCSA8	H25
MISC	
VCCSA_SENSE	H23
VCCSA_VID0	C22
VCCSA_VID1	C24
VCCIO_SEL	A19

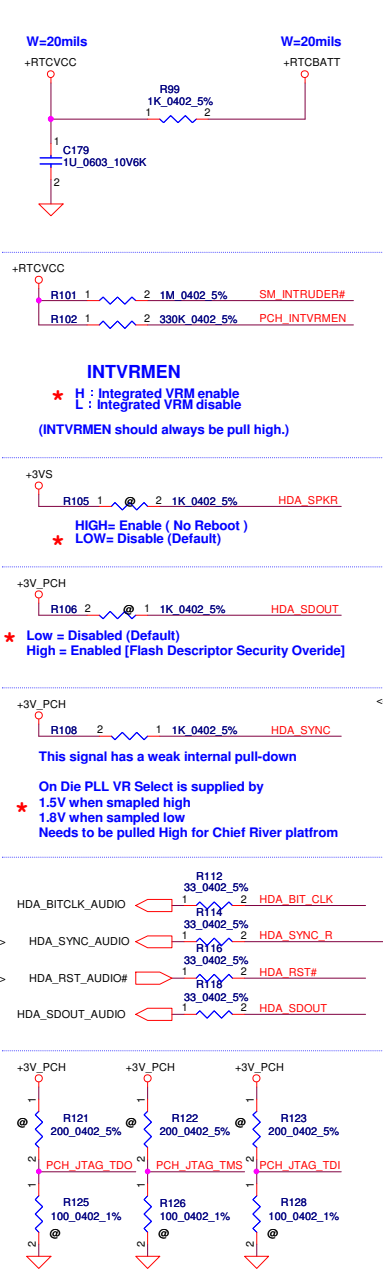


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**INTRVMEN**

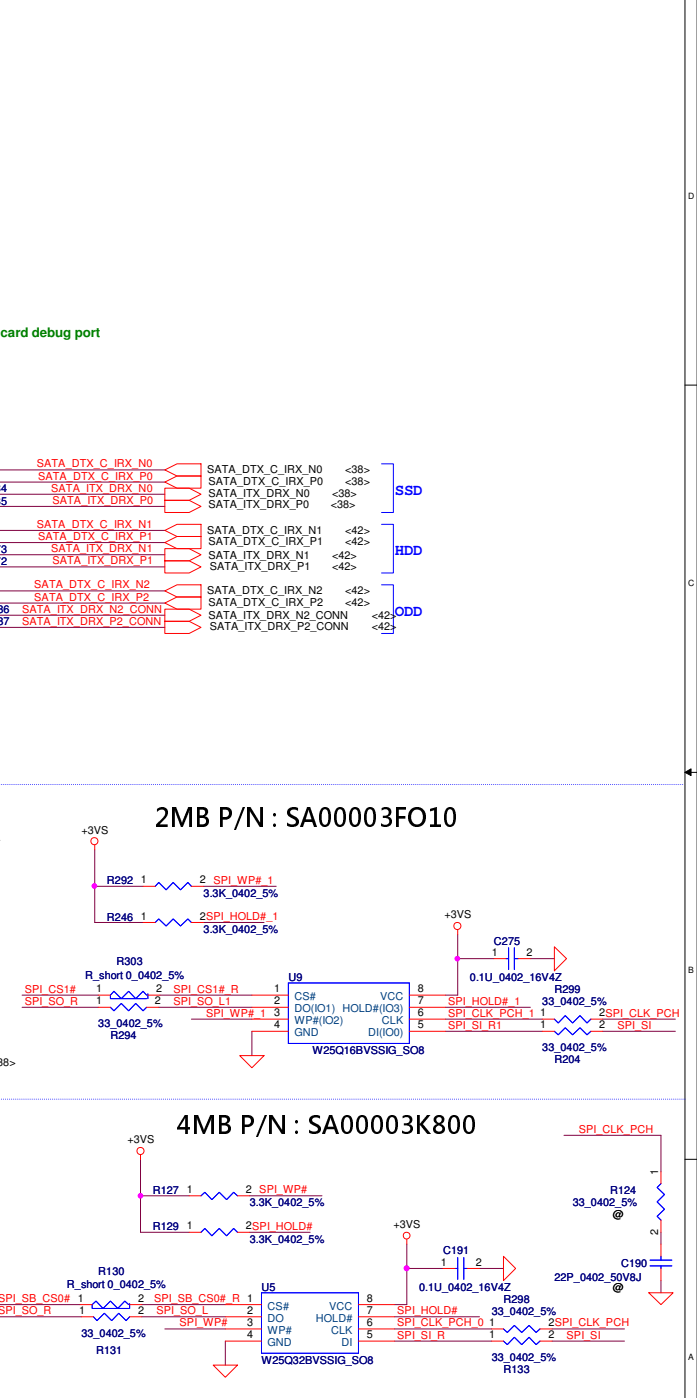
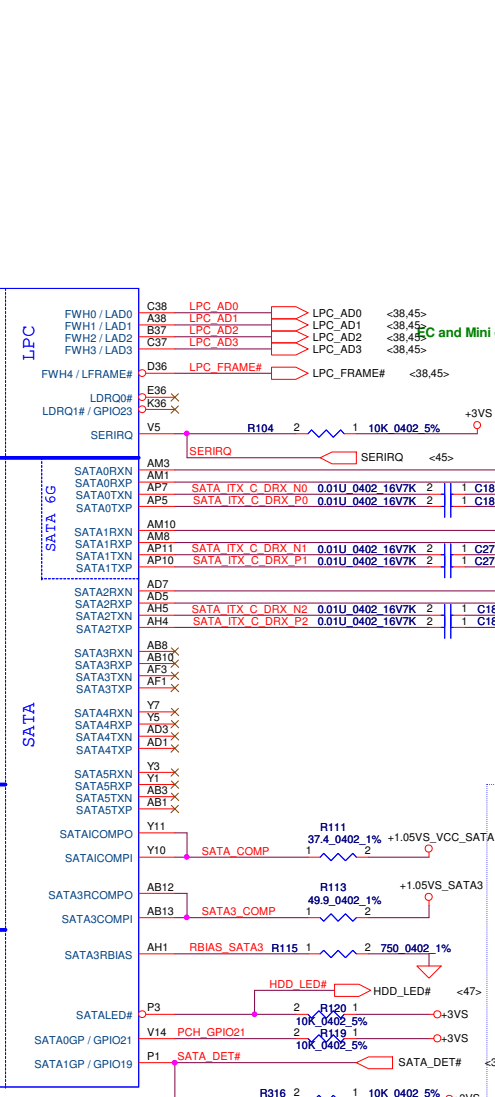
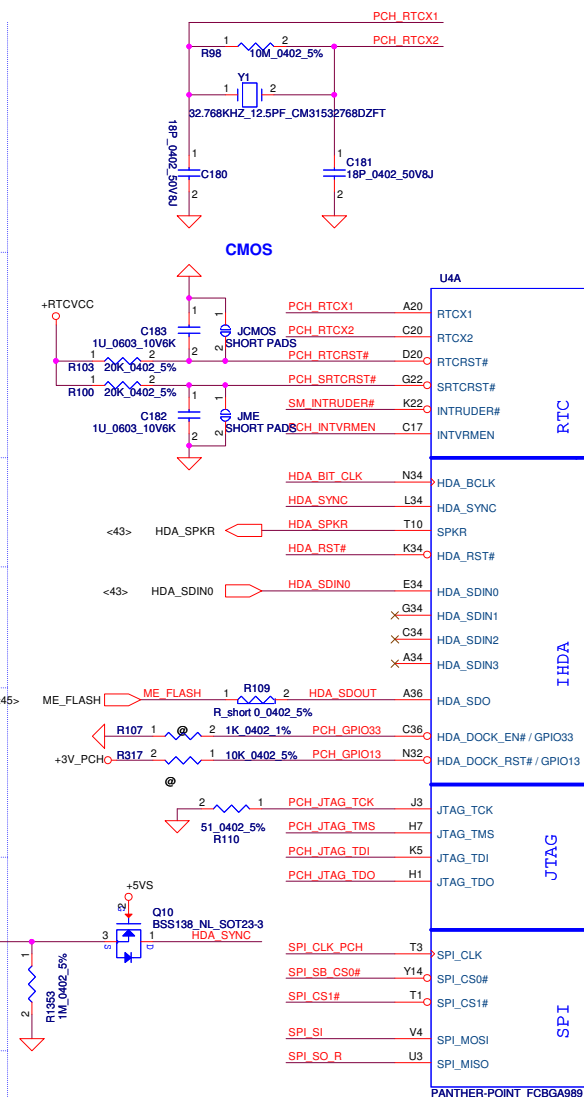
H : Integrated VRM enable  
L : Integrated VRM disable

(INTRVMEN should always be pull high.)

HIGH= Enable (No Reboot)  
LOW= Disable (Default)

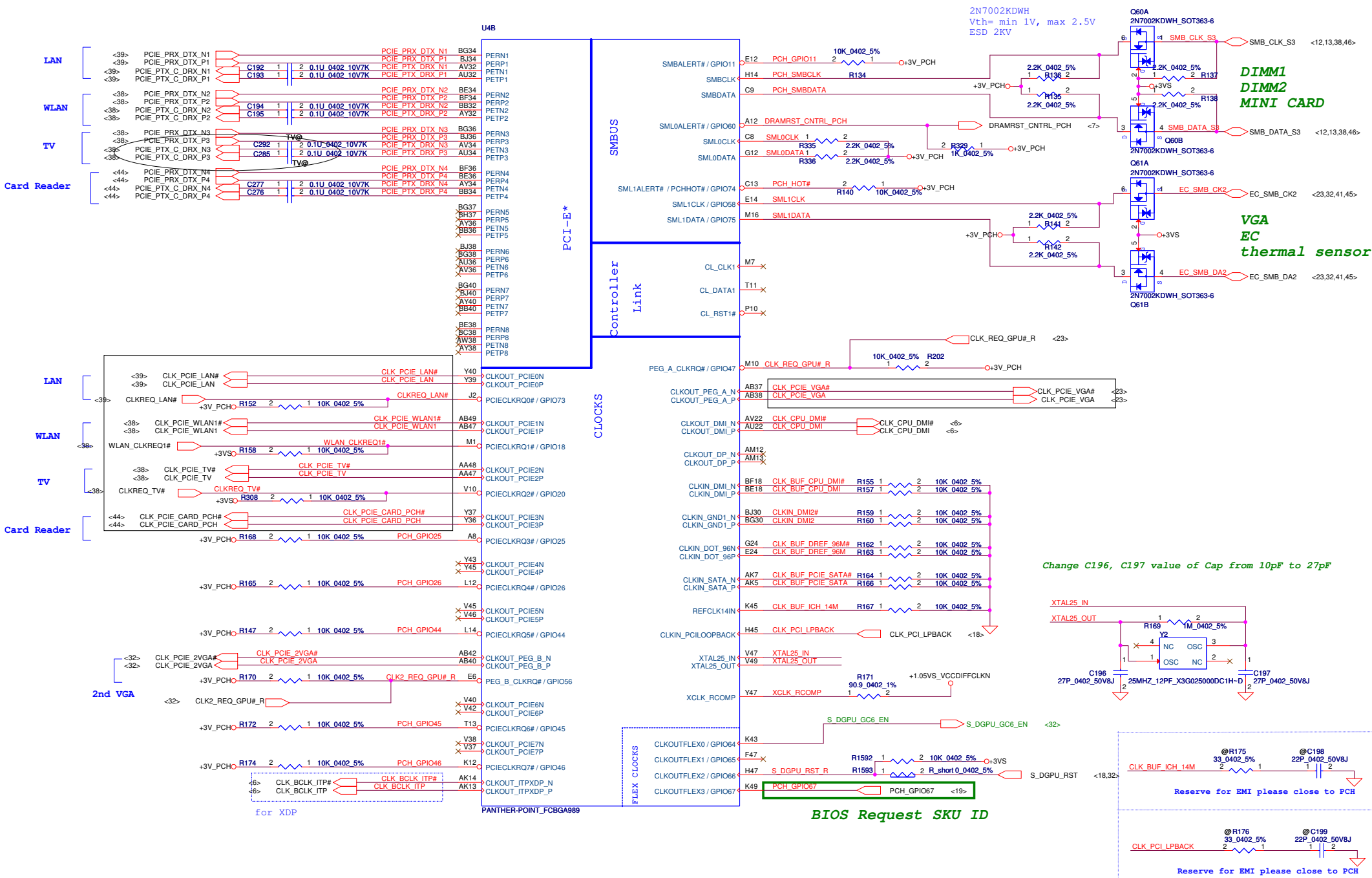
Low = Disabled (Default)  
High = Enabled (Flash Descriptor Security Override)

On Die PLL VR Select is supplied by 1.5V when sampled high 1.8V when sampled low Needs to be pulled High for Chief River platform



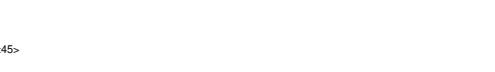
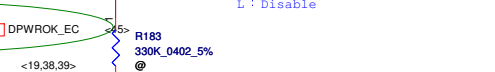
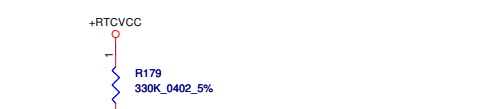
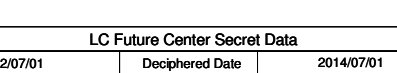
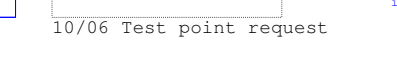
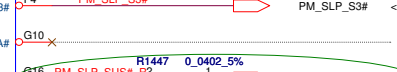
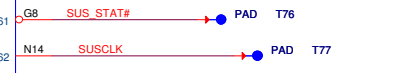
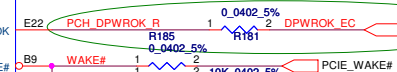
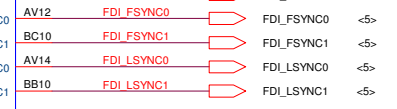
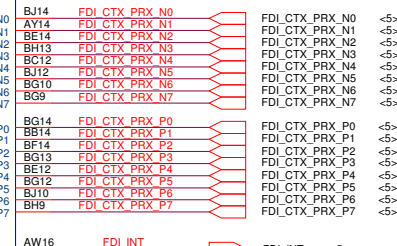
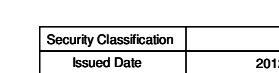
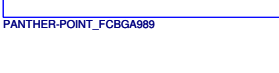
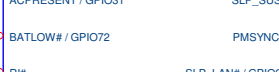
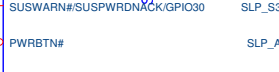
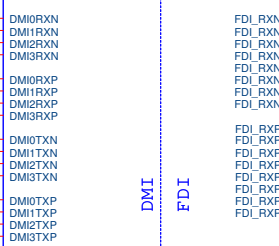
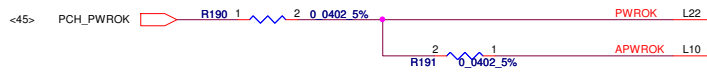
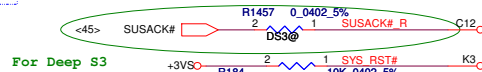
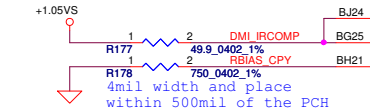
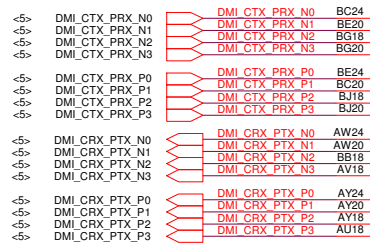
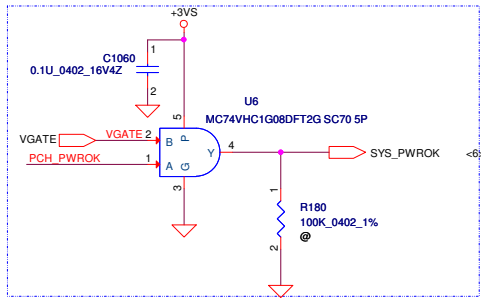
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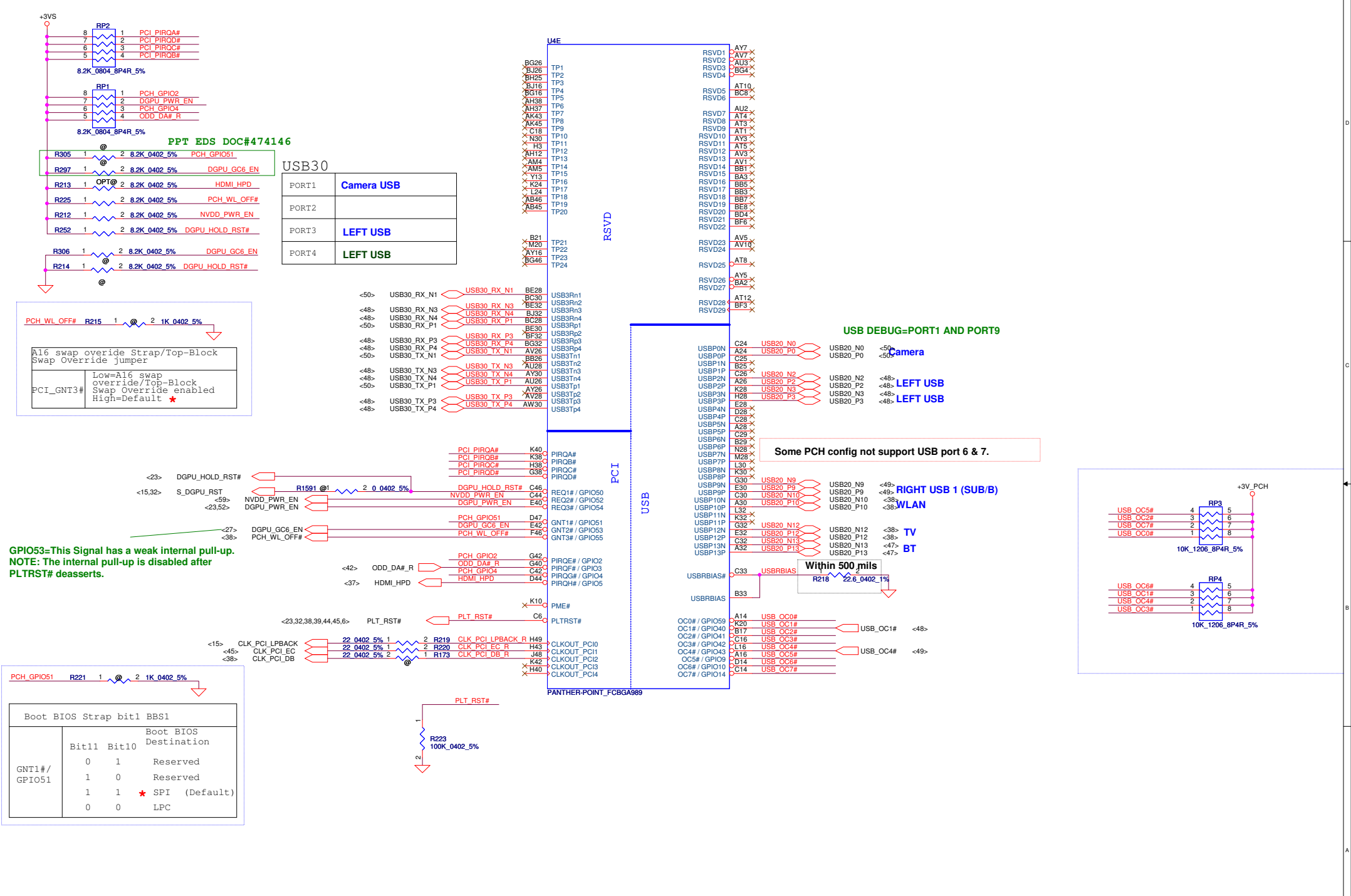
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Issued Date		2012/07/01		Deciphered Date		2014/07/01		PCH (2/9) PCIE, SMBUS, CLK							
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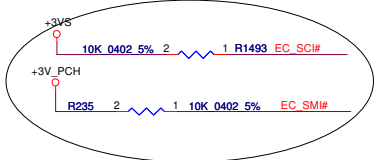




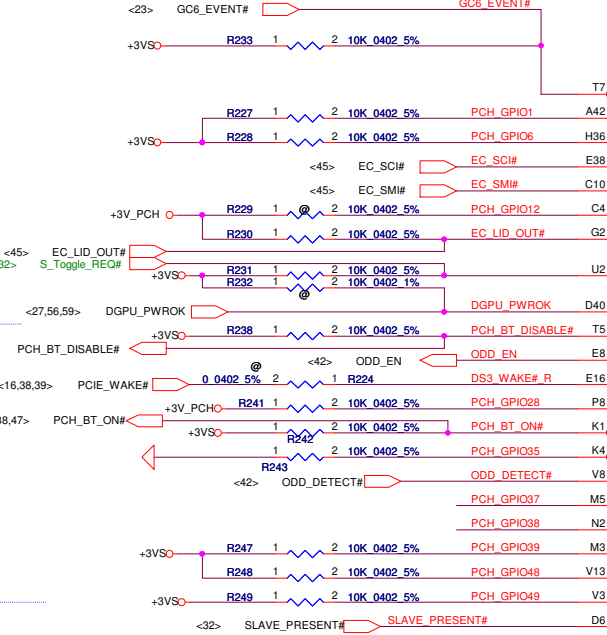
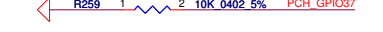
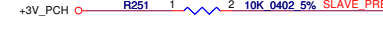
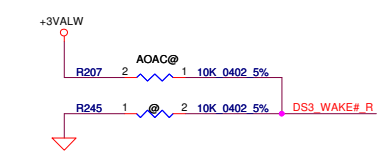




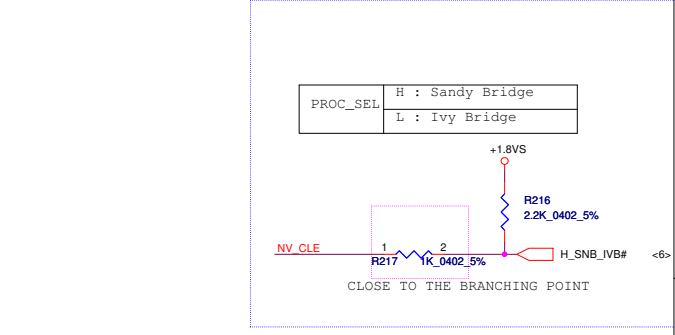
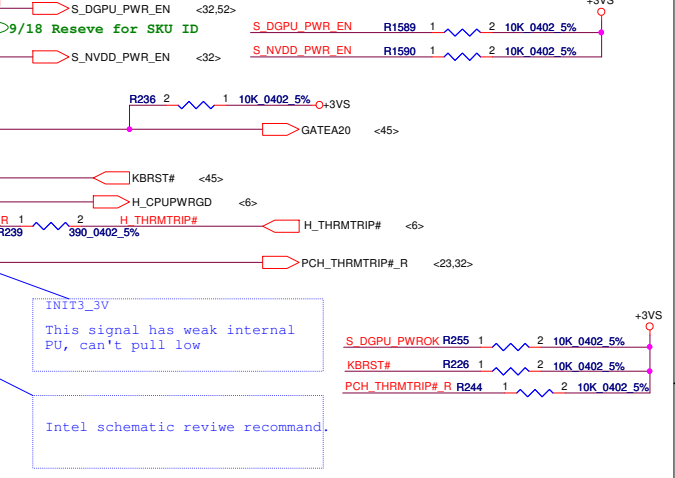
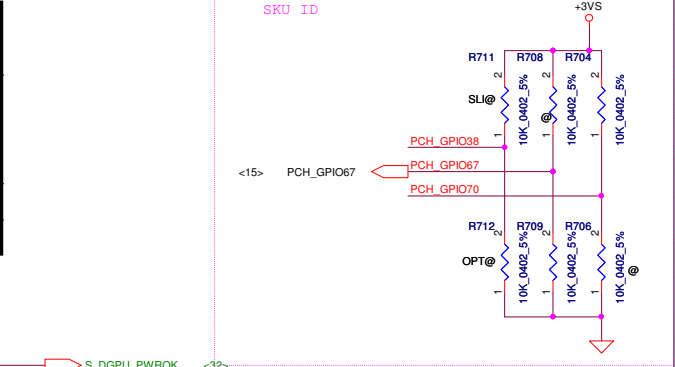
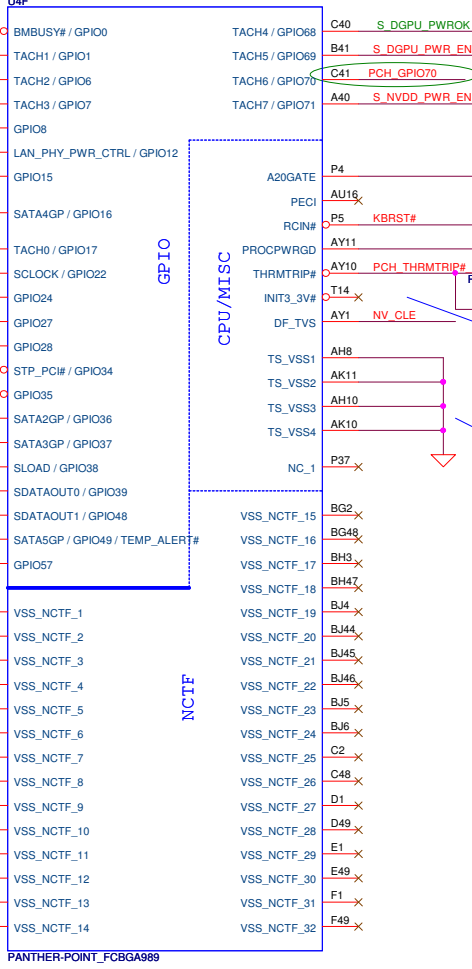


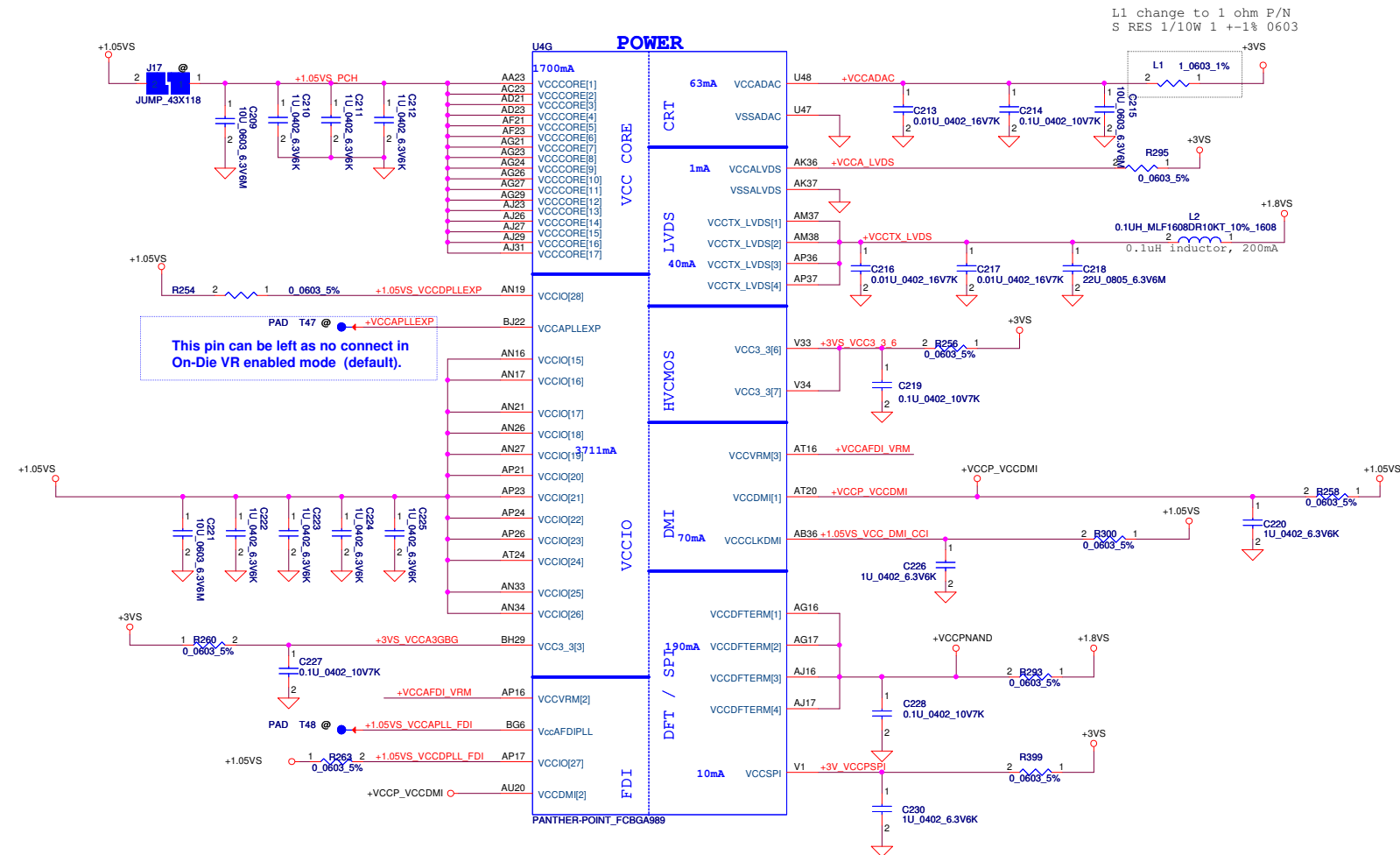


**GPIO28**  
On-Die PLL Voltage Regulator  
This signal has a weak internal pull up  
★ H : On-Die voltage regulator enable  
L : On-Die PLL Voltage Regulator disable

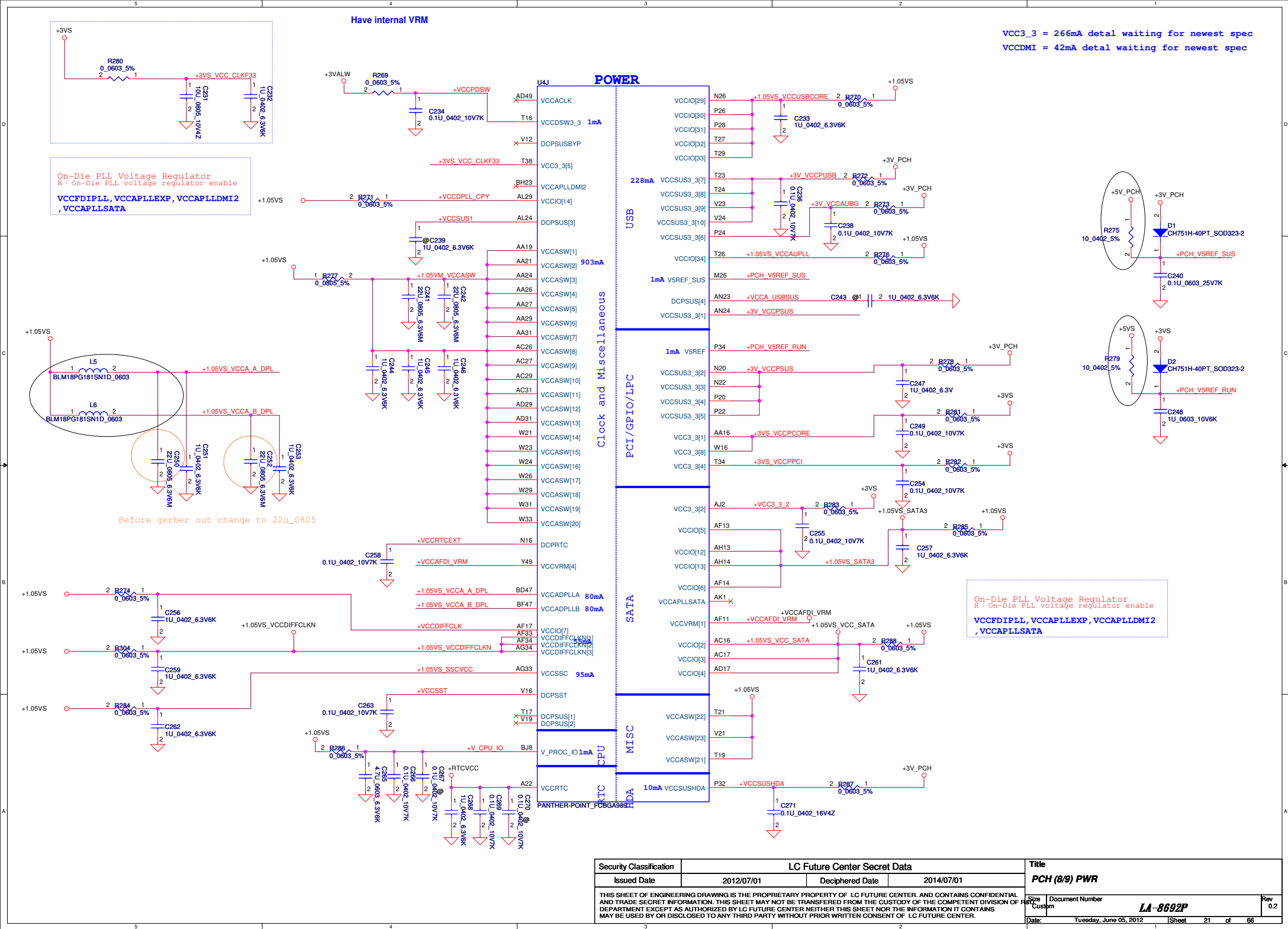


Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
Optimus	0	0	X
Reserve	0	1	X
DIS (SLI)	1	0	X
Reserve	1	1	X
14"	X	X	0
15"	X	X	1





Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.05	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTerm	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

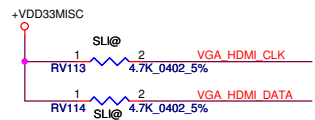


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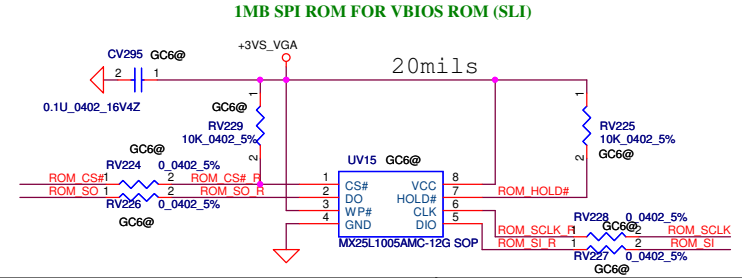
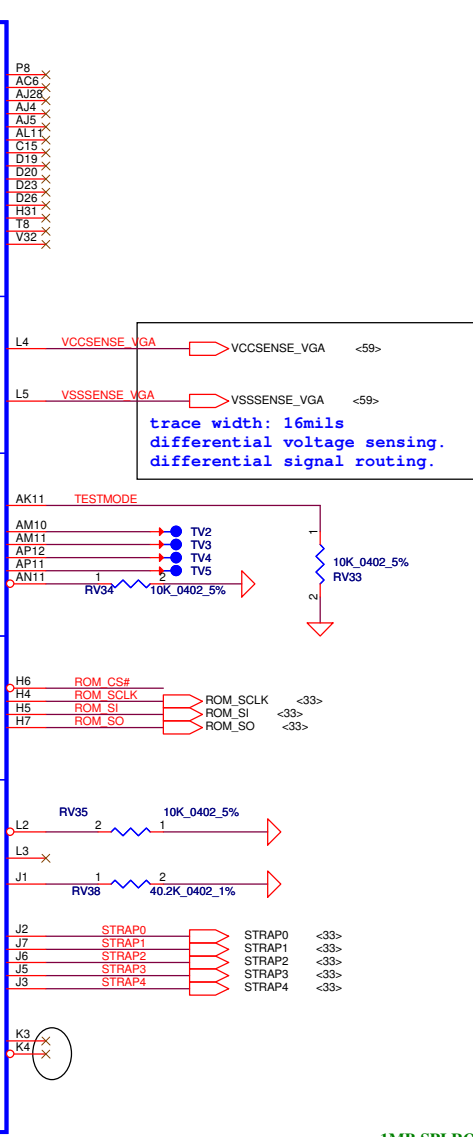
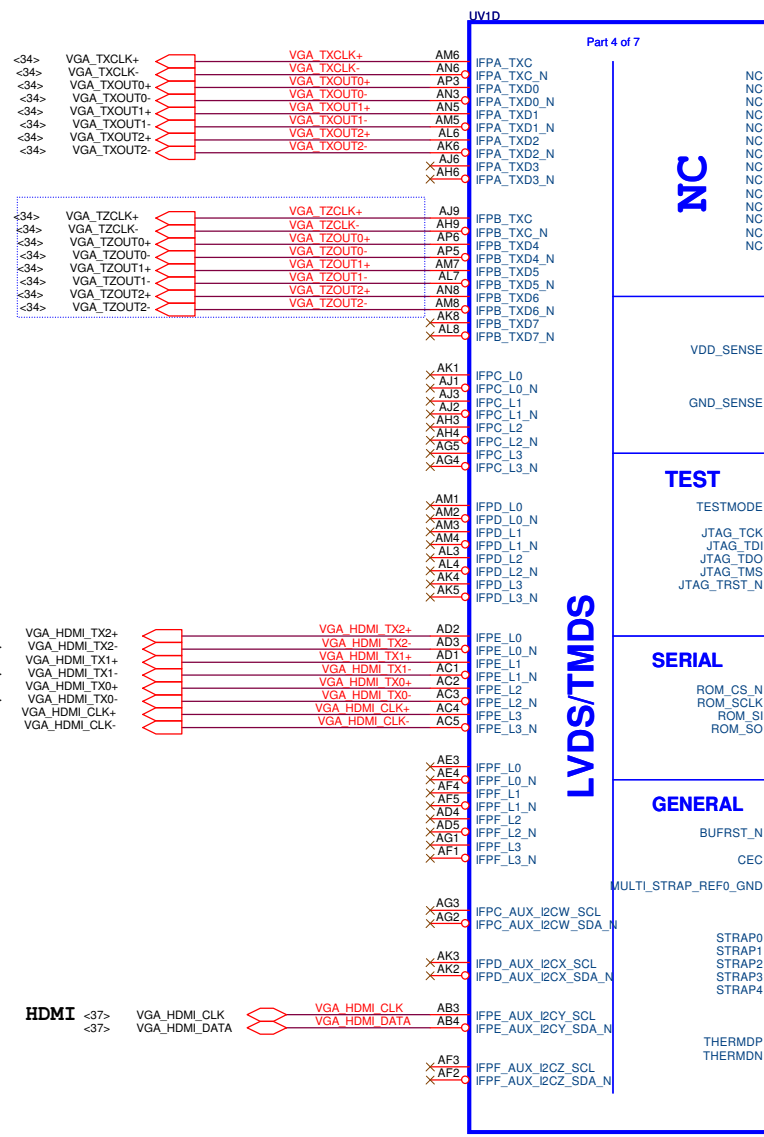
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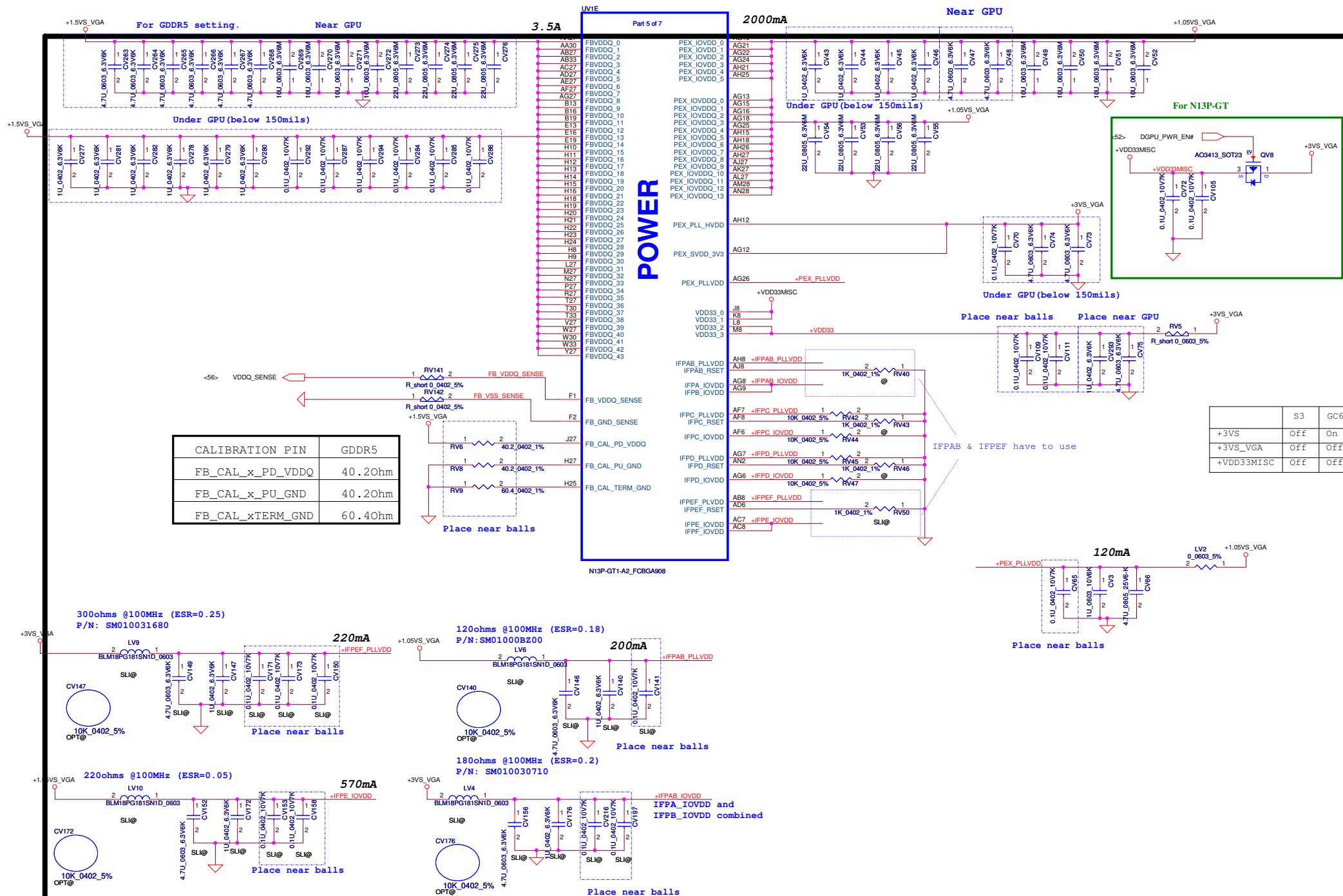


for 15" dual channel



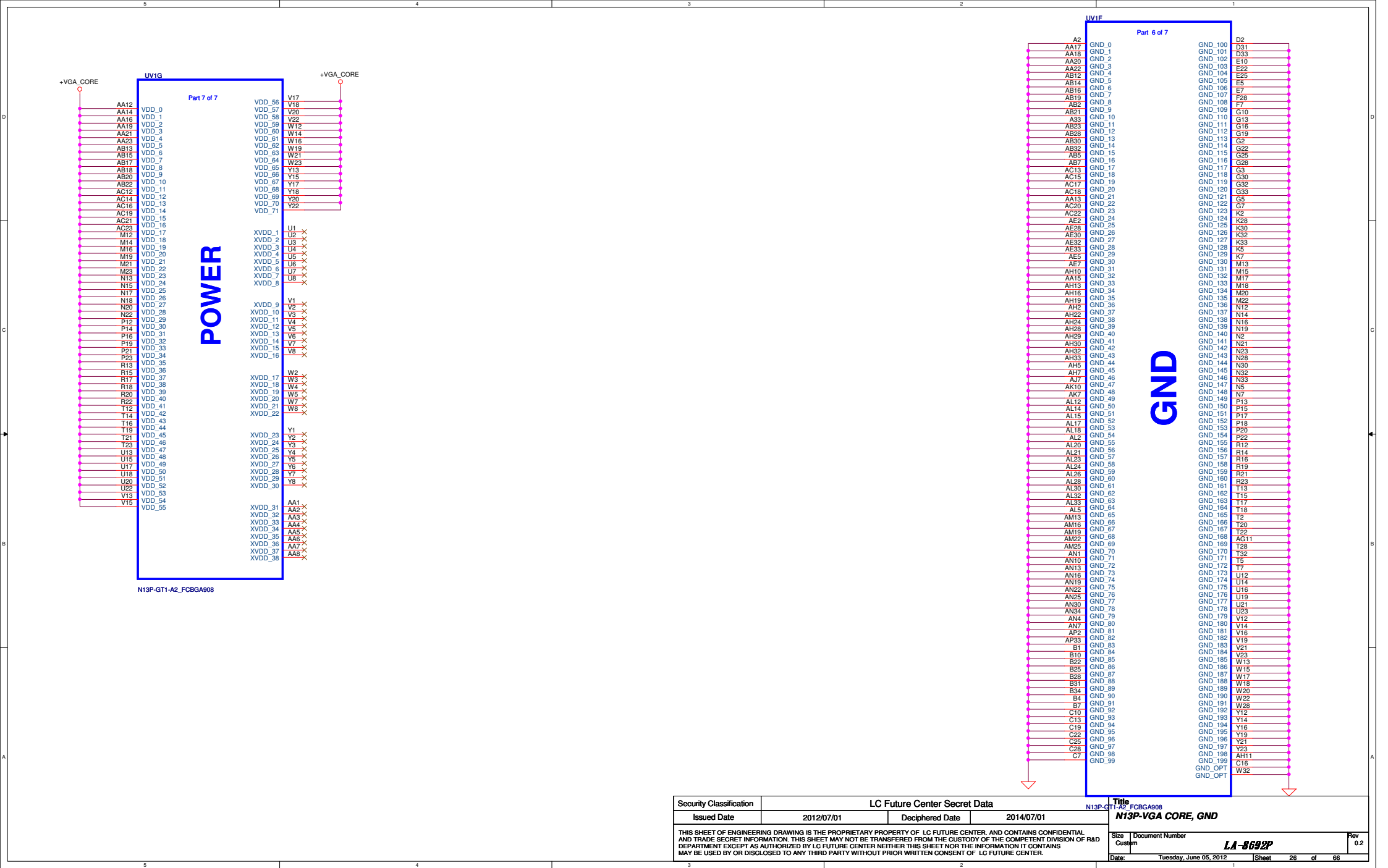
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Issued Date		2012/07/01		Deciphered Date		2014/07/01		N13P-LVDS/HDMI/DP/THM			
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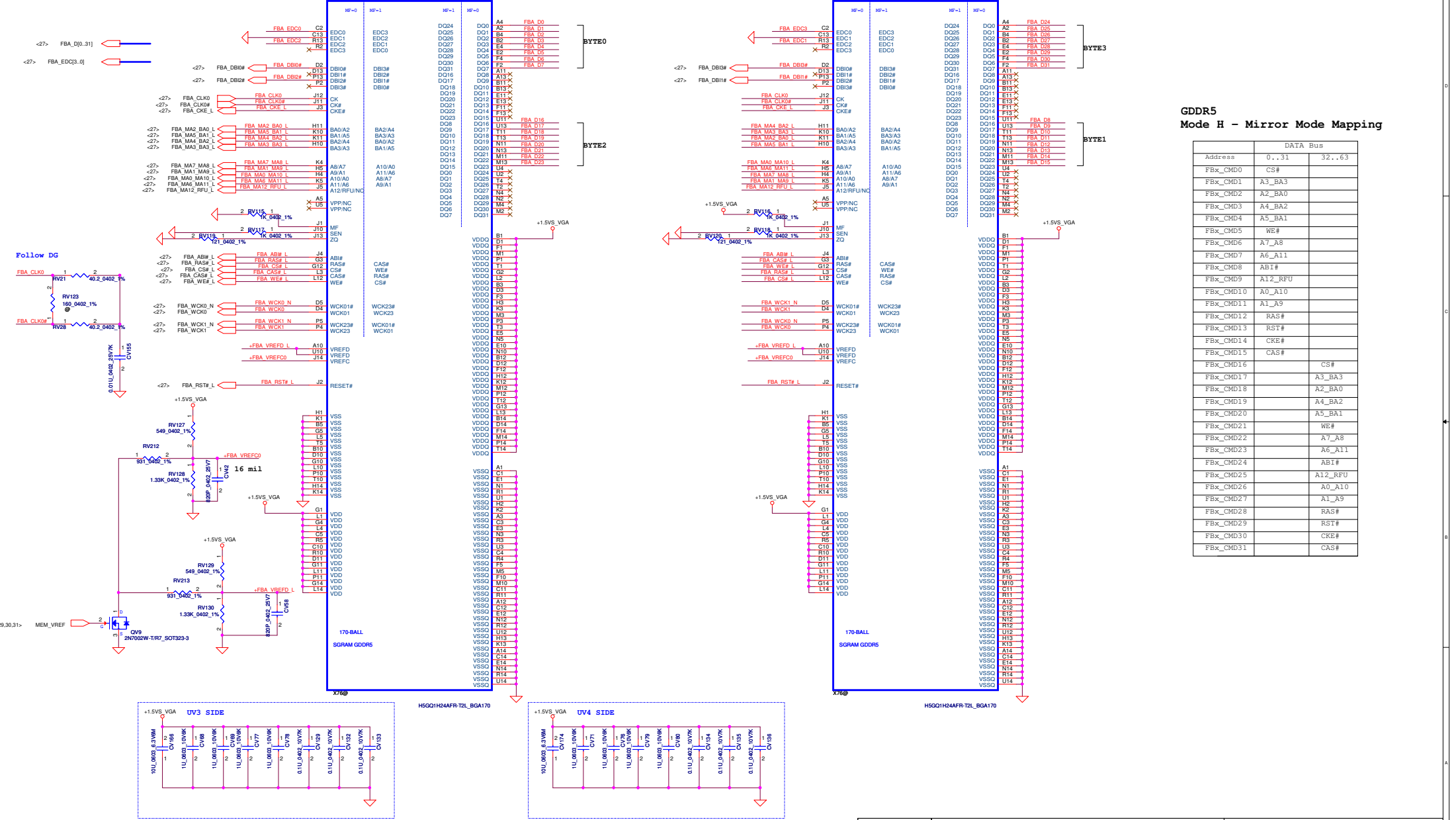
CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.20hm
FB_CAL_x_PU_GND	40.20hm
FB_CAL_x_TERM_GND	60.40hm

	S3	GC6
+3VS	Off	On
+3VS_VGA	Off	Off
+VDD33MISC	Off	Off

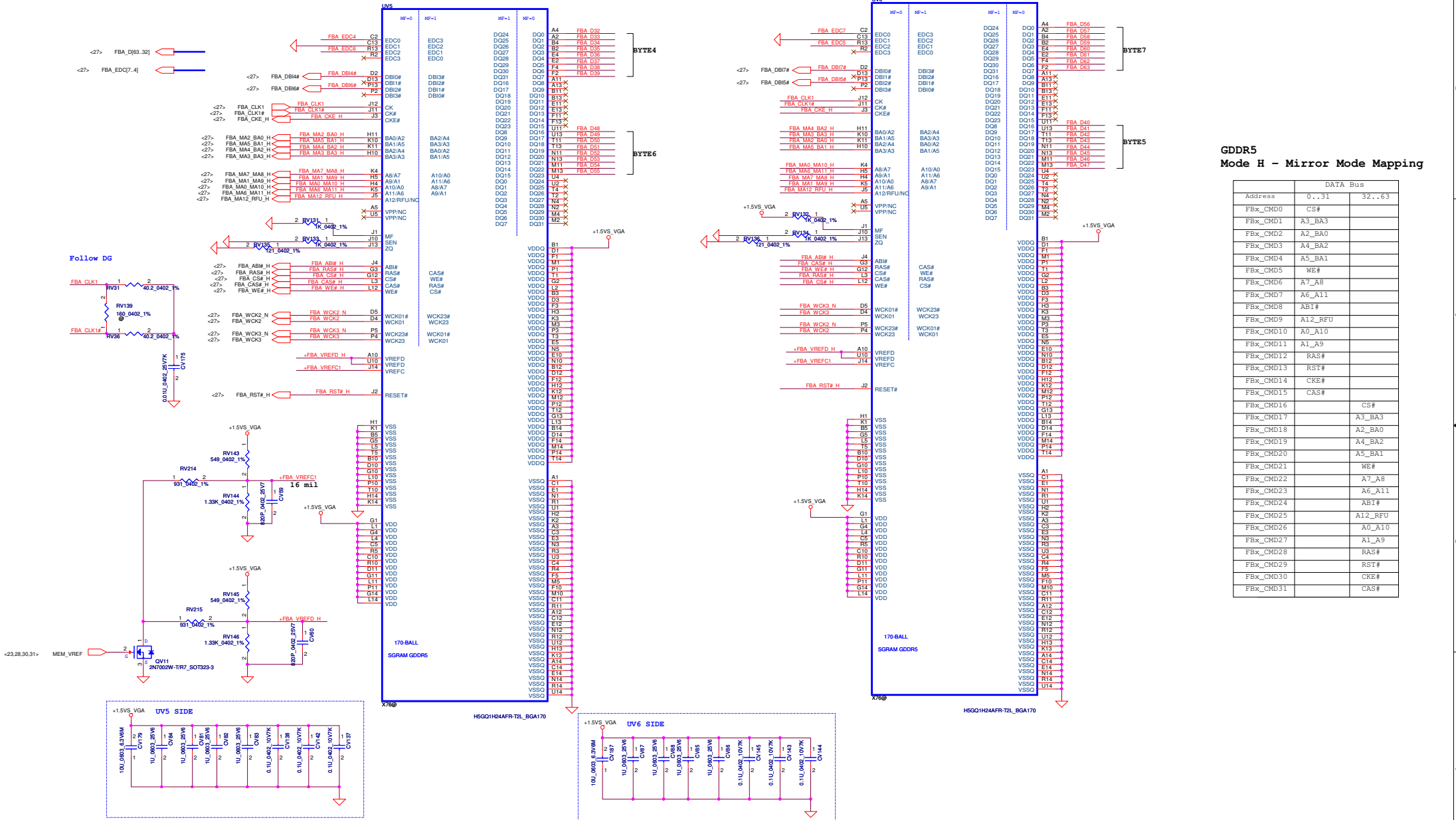




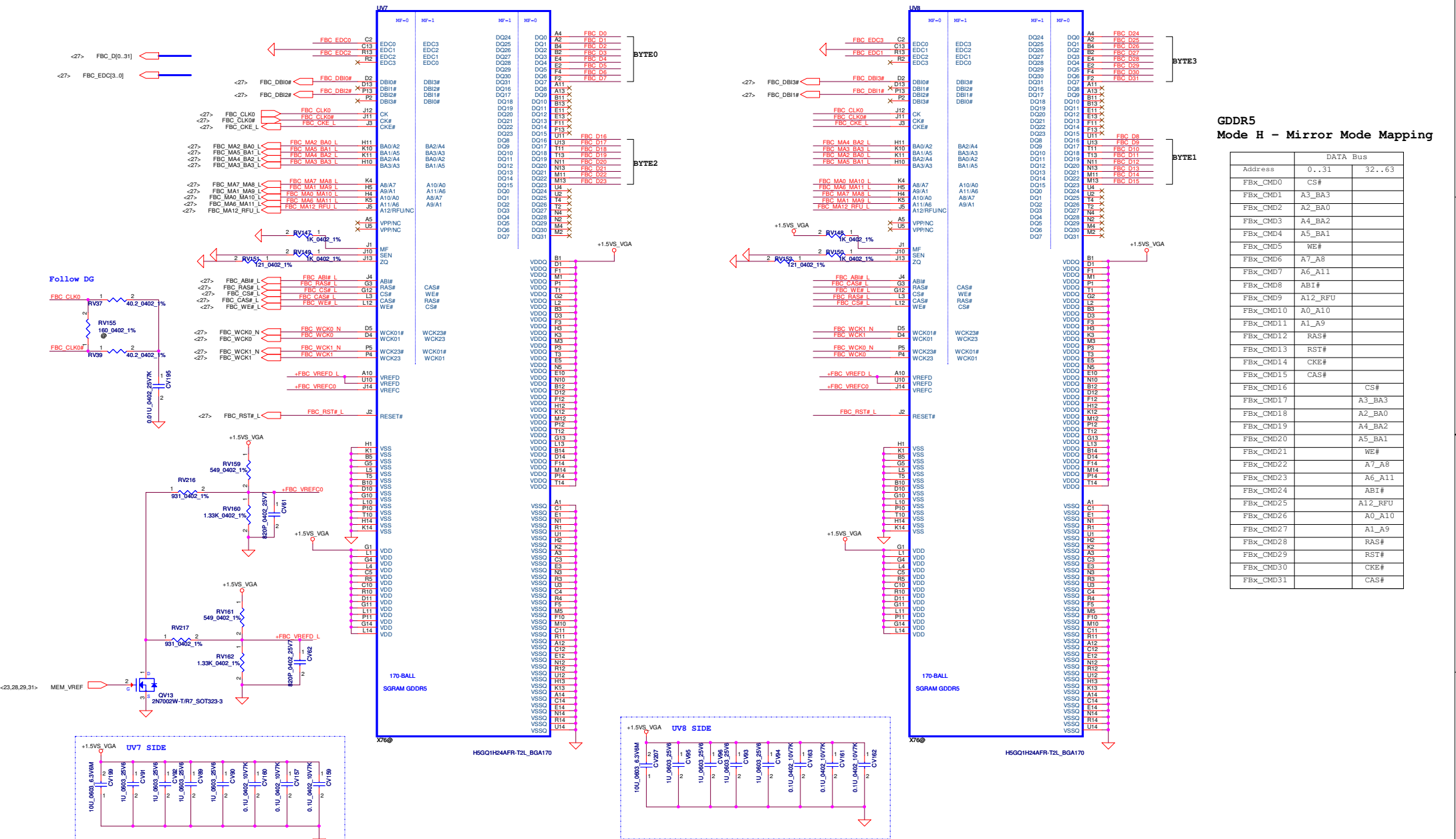
Memory - Lower 32 bits



Memory - Upper 32 bits



Memory Partition C - Lower 32 bits

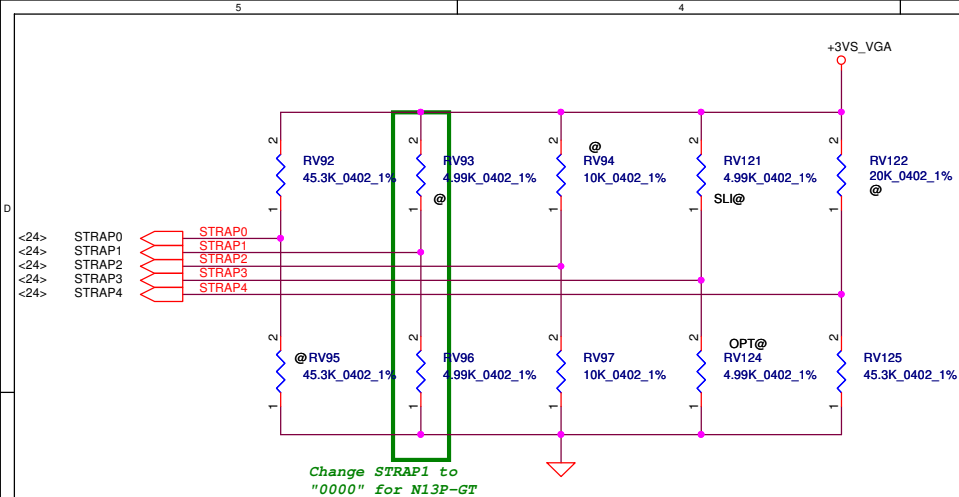




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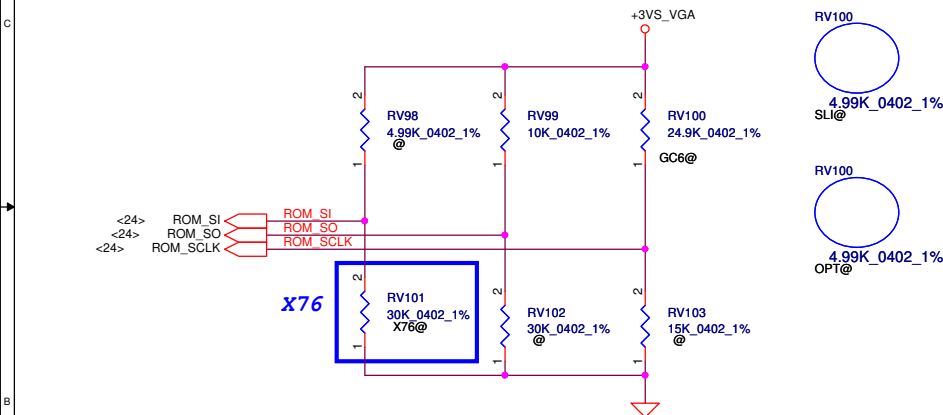






Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



				X76								
GPU	FB Memory (GDDR5)			ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	Samsung	K4G20325FD-FC04	2G	PD 30K	PU 10K	PU 25K GC6@	PU 45K	PD 5K	PD 10K	PU 5K SLI@	PD 45K	64Mx32
		K4G10325FG-HC04	1G	PD 45K								32Mx32
	Hynix	H5GQ2H24AFR-T2C	2G	PD 25K	PU 5K OPT@, SLI@	PD 5K OPT@	64Mx32					
		H5GQ1H24BFR-T2C	1G	PD 35K			32Mx32					

3GIO_PADCFG		XCLK_417	
3GIO_PADCFG[3:0]		0	277MHz (Default)
0000	Notebook Default	1	Reserved

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

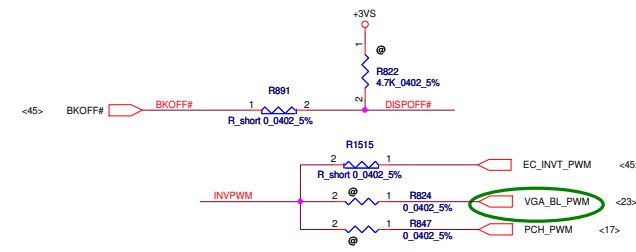
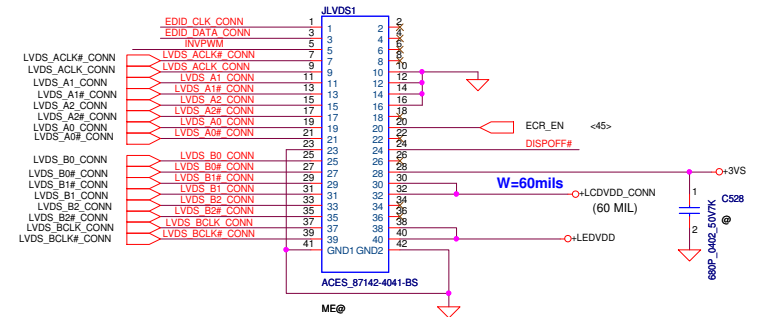
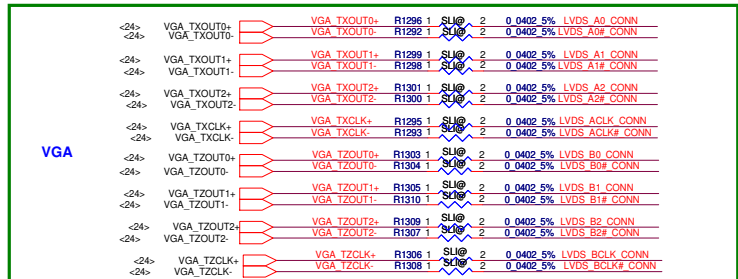
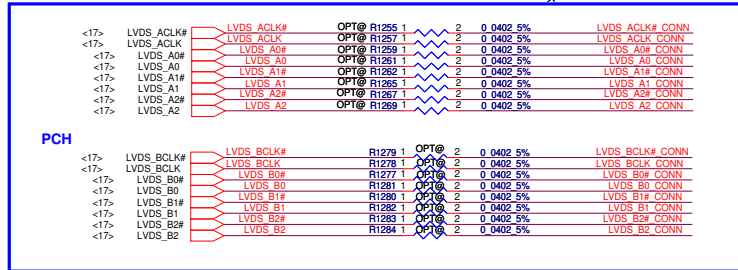
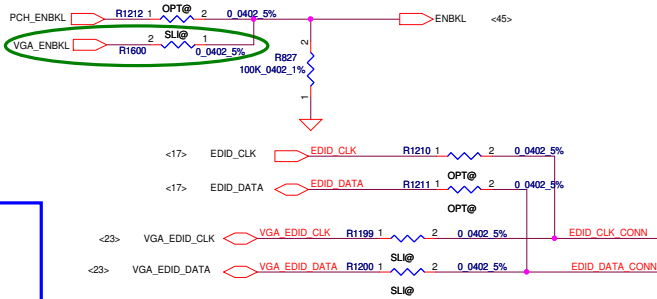
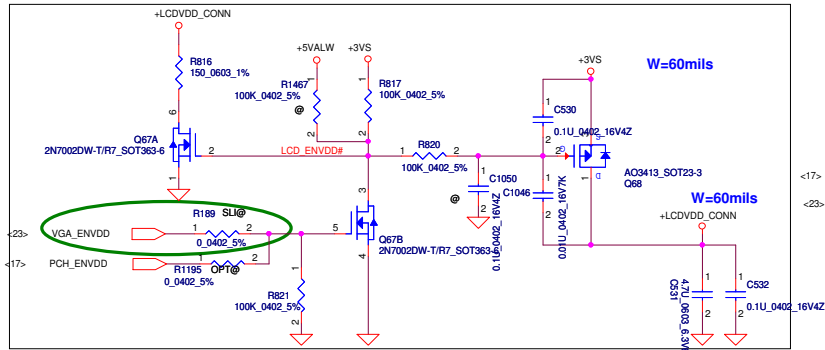
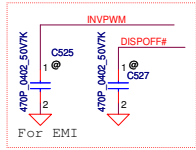
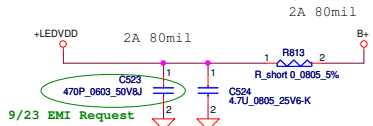
USER Straps	
User[3:0]	
1000-1100	Customer defined

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

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				Date: Thursday, June 07, 2012
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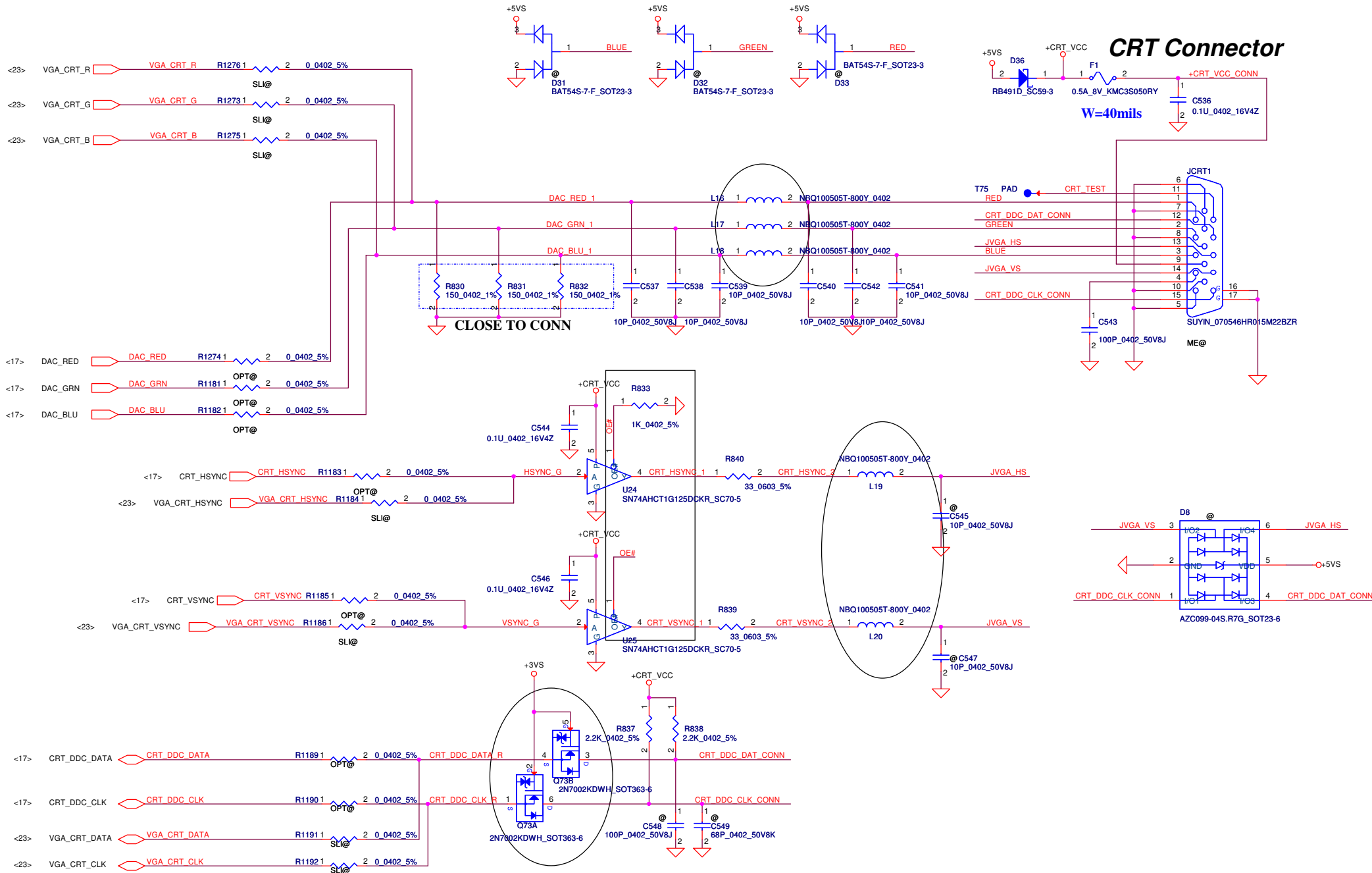


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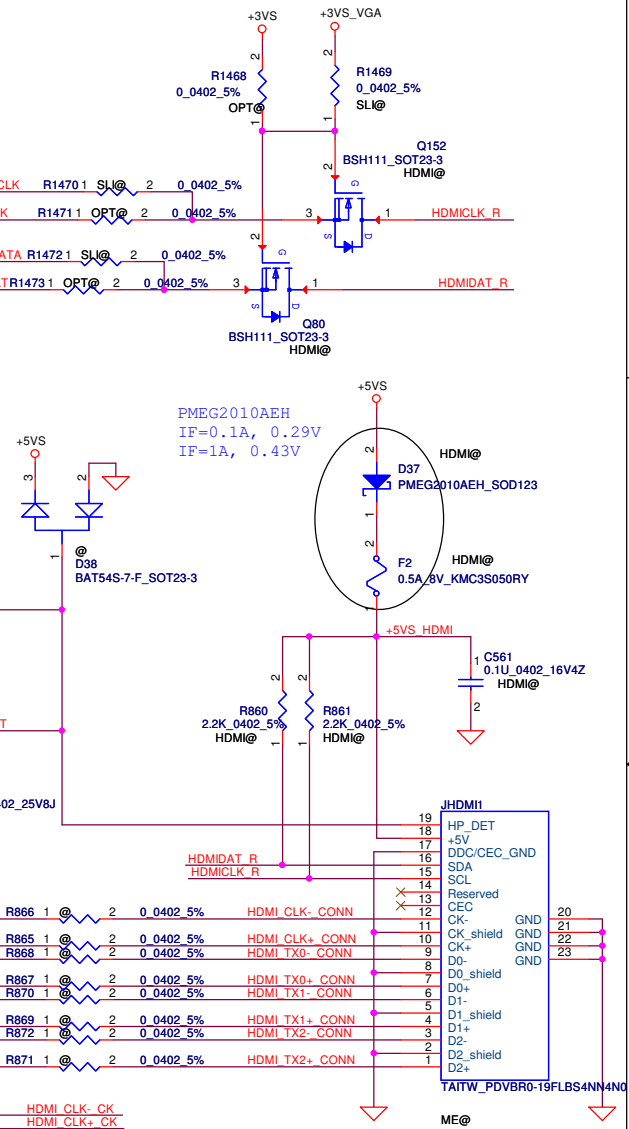
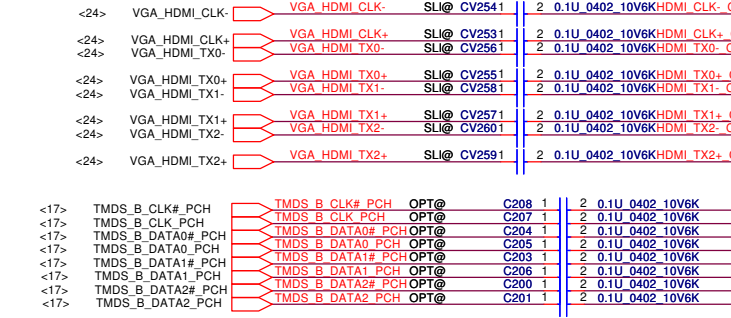
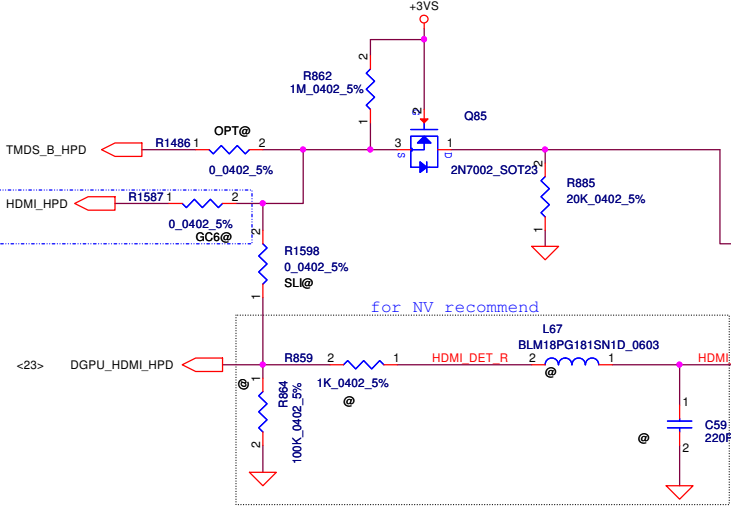
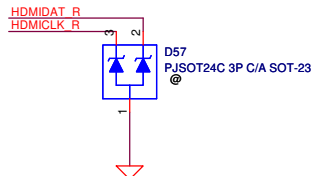
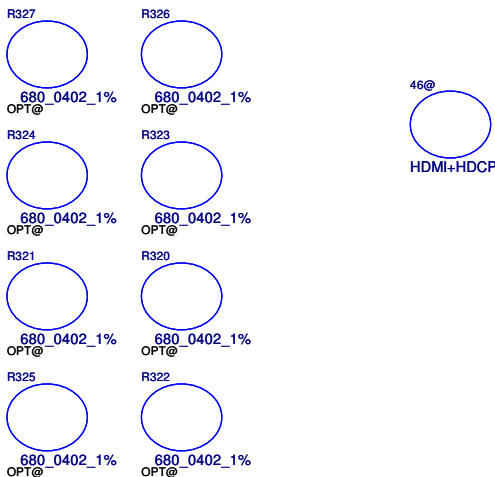
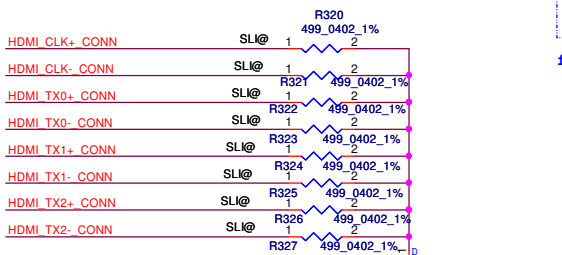
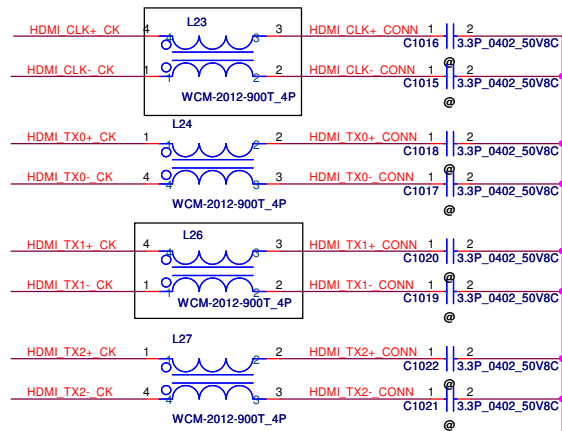
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No use NVSR chip for DVT

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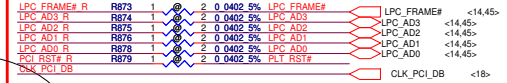
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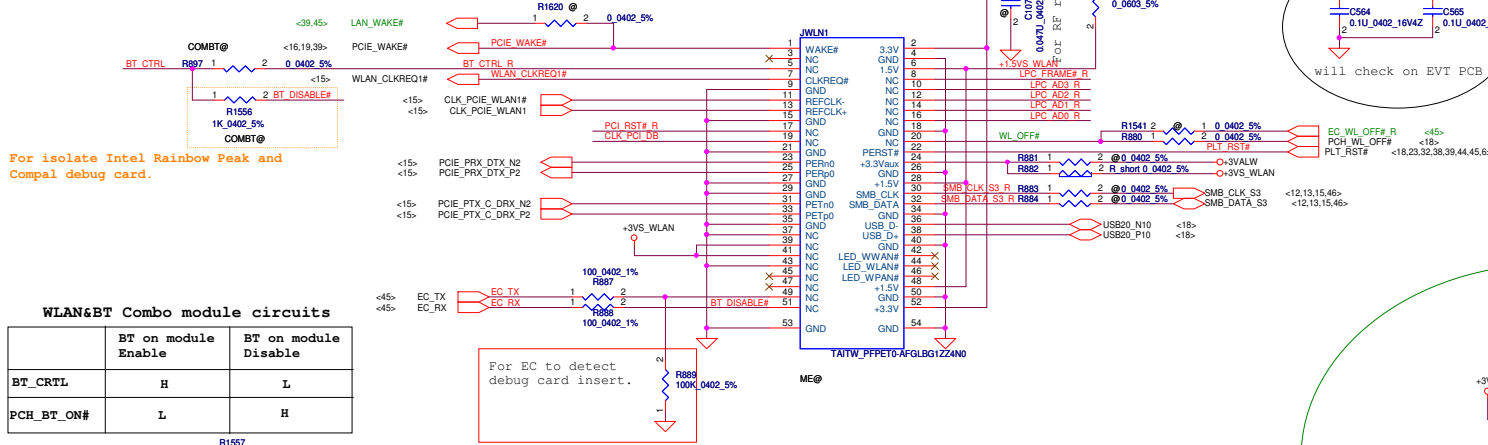
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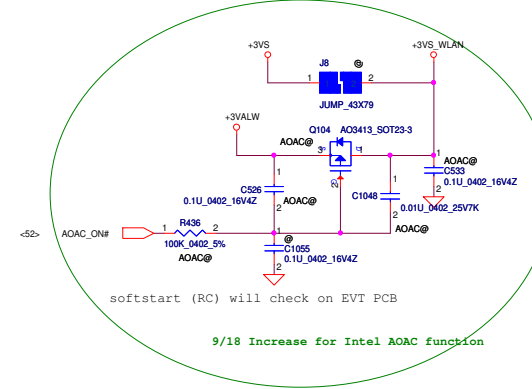
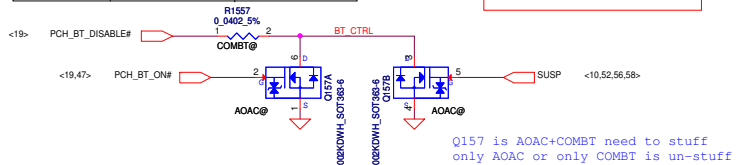
Reserve for SW mini-pcie debug card.  
Series resistors closed to KBC side.



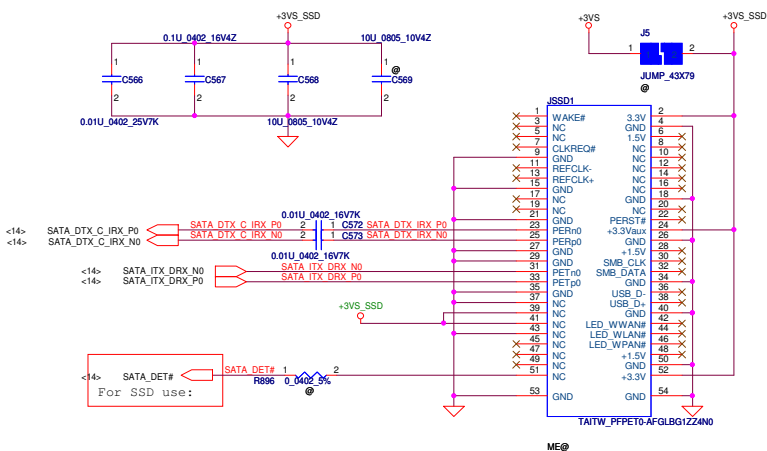
For isolate Intel Rainbow Peak and Compal debug card.



	BT on module Enable	BT on module Disable
BT_CTRL	H	L
PCH_BT_ON#	L	H



## SSD Active:4.5W(1.5A)

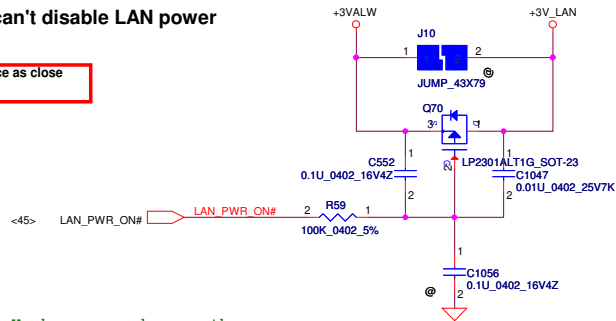


Pinout diagram for the TAITW\_PFPETO-AFGLBG124N0 component. The diagram shows a 54-pin package with various signals and power connections. Signals include CLKREQ\_TV#, CLK\_PCIE\_TV#, CLK\_PCIE\_TV, POE\_PRX\_DTX\_N3, POE\_PRX\_DTX\_P3, POE\_PTX\_C\_DRX\_N3, POE\_PTX\_C\_DRX\_P3, PLT\_RST#, USB20\_N12, and USB20\_P12. Power connections include +3VS\_TV, +1.5VS\_TV, +3VS\_TV, +1.5VS\_TV, and +3VS\_TV. The diagram also shows the internal structure of the component, including the TAITW\_PFPETO-AFGLBG124N0 chip and the TAITW\_PFPETO-AFGLBG124N0 chip.

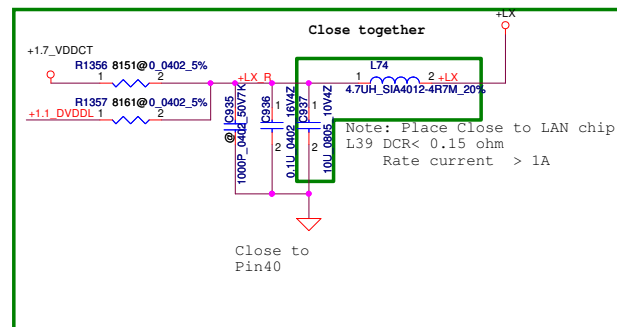
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Issued Date		2012/07/01	Deciphered Date	2014/07/01	Mini-Card
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## Atheros request can't disable LAN power

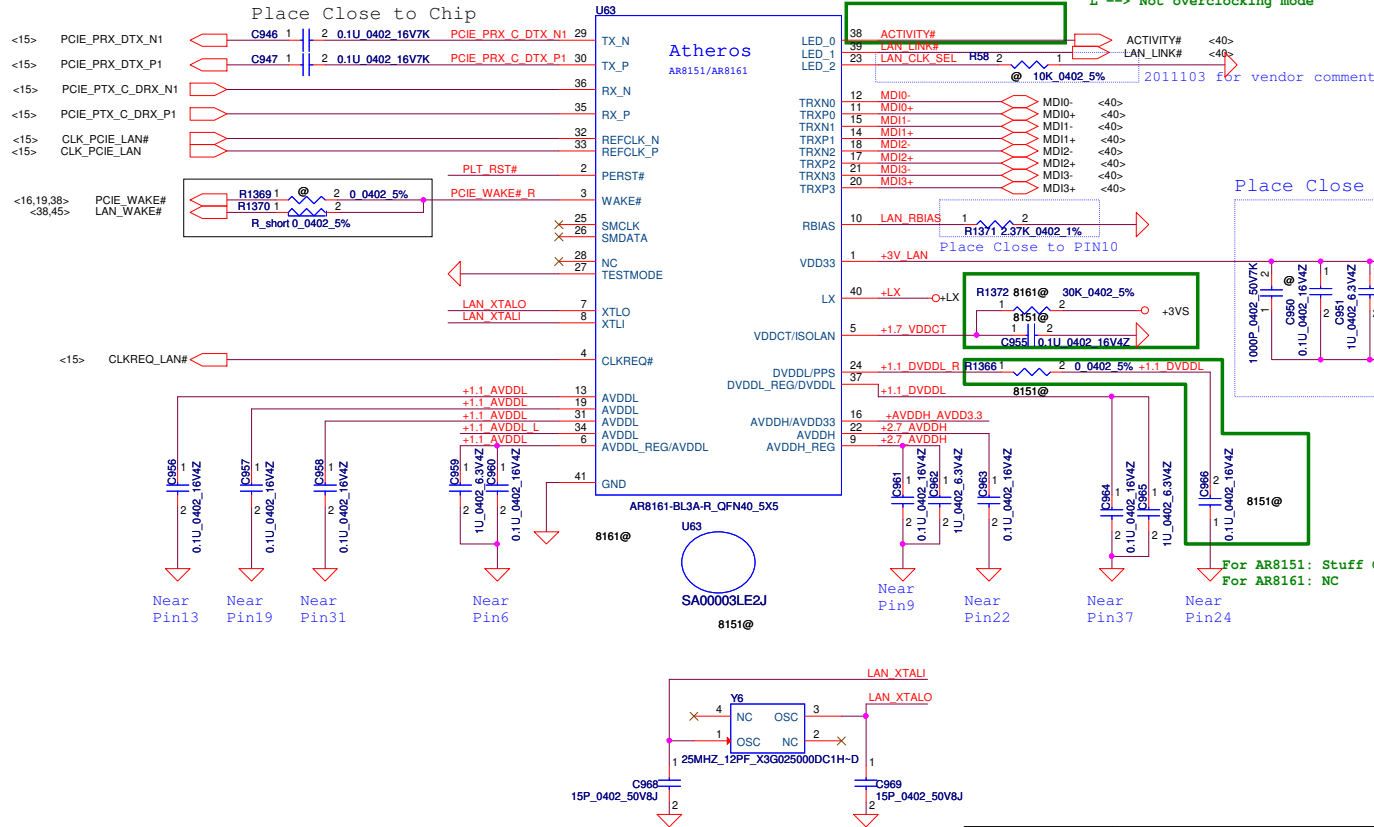
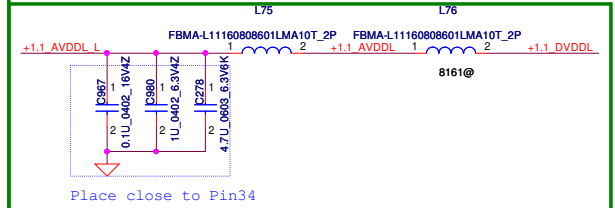
**Layout Notice : Place as close  
chip as possible.**



Vendor recommend reseve the  
PU resistor close LAN chip

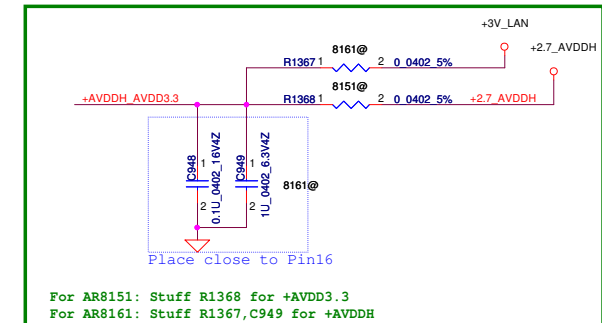
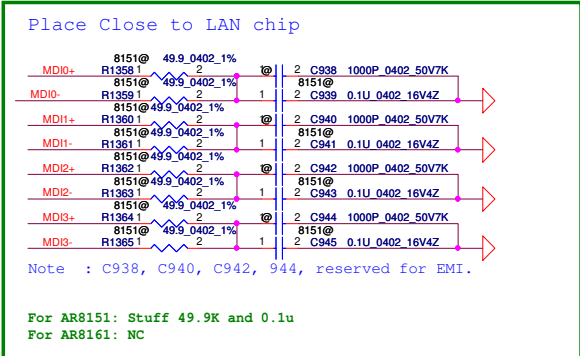


	LX Voltage <Pin 40>	Configure
AR8151	+1.7V <VDDCT>	R1356, C955
AR8161	+1.1V <DVDDL, AVDDL>	R1357, R1372, L76



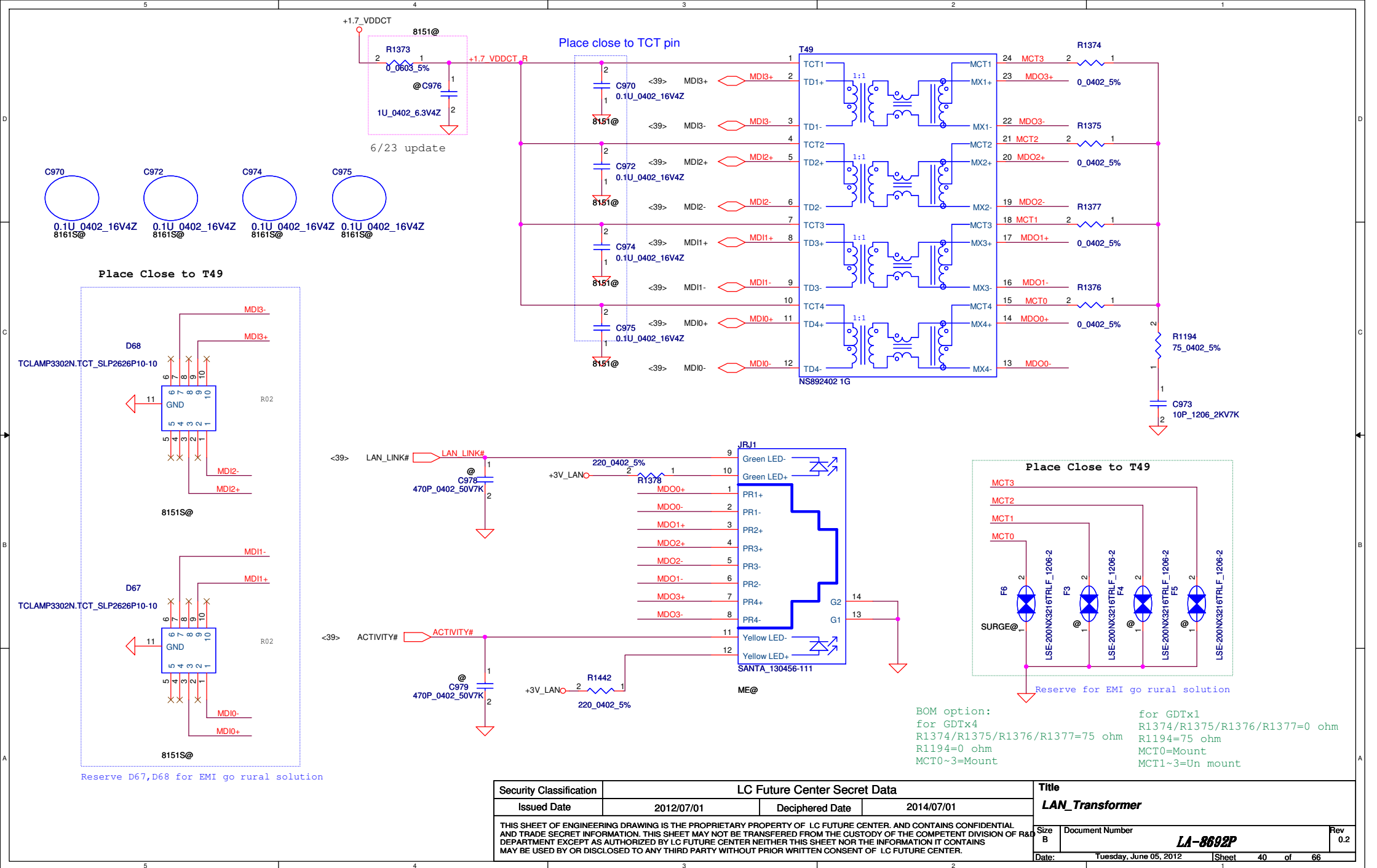
```
H --> Overclocking mode
L --> Not overclocking mode
```

Place Close to PIN1

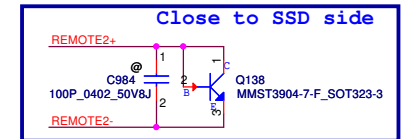
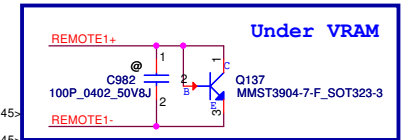
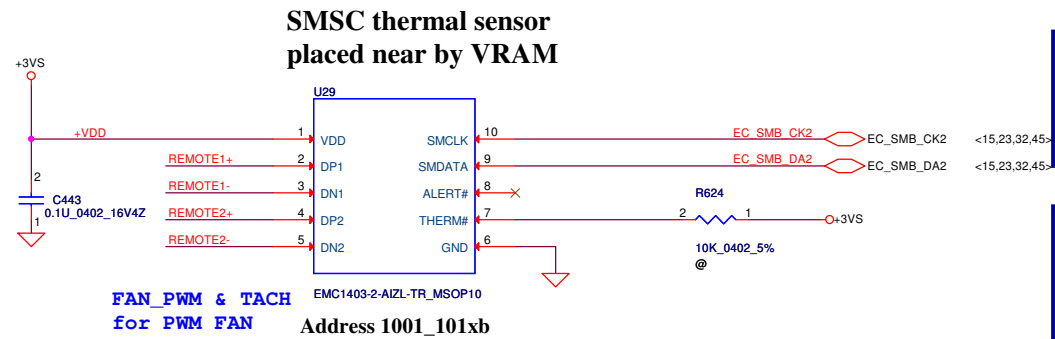
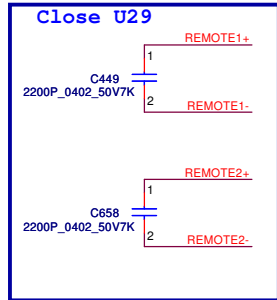


Change C968, C969 value of Cap from 33pF to 15pF  
for TXC recommend

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				Custom	LA-8602P	0.2
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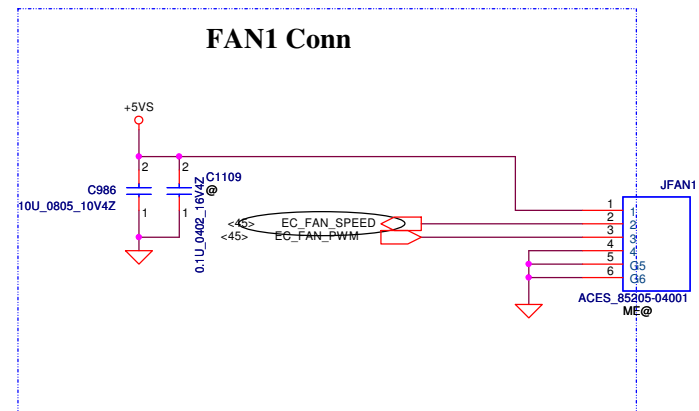






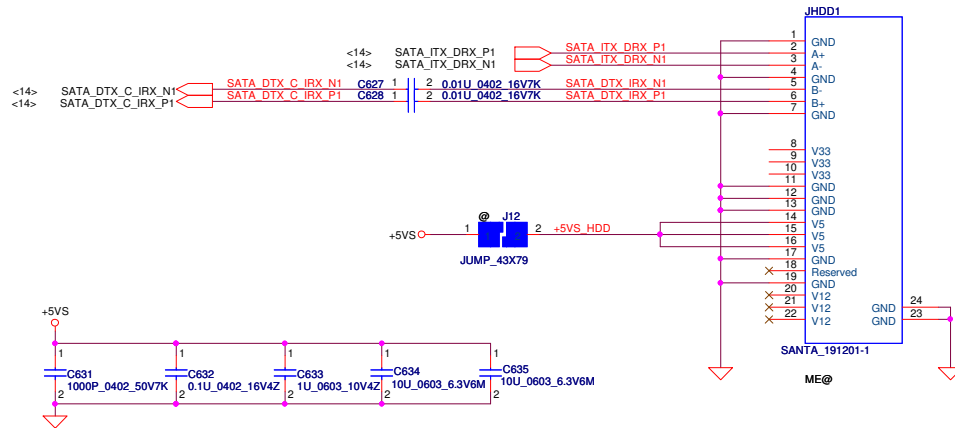
internal pull up 1.2K to 1.5V  
R for initial thermal  
shutdown temp

REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"

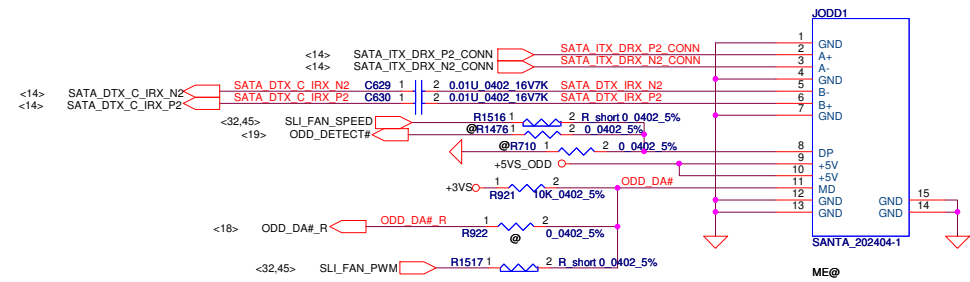


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				Rev	0.2
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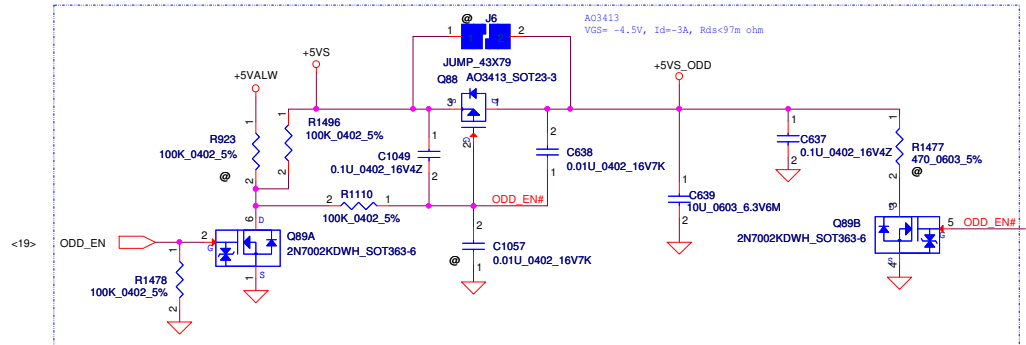
## SATA HDD Conn.



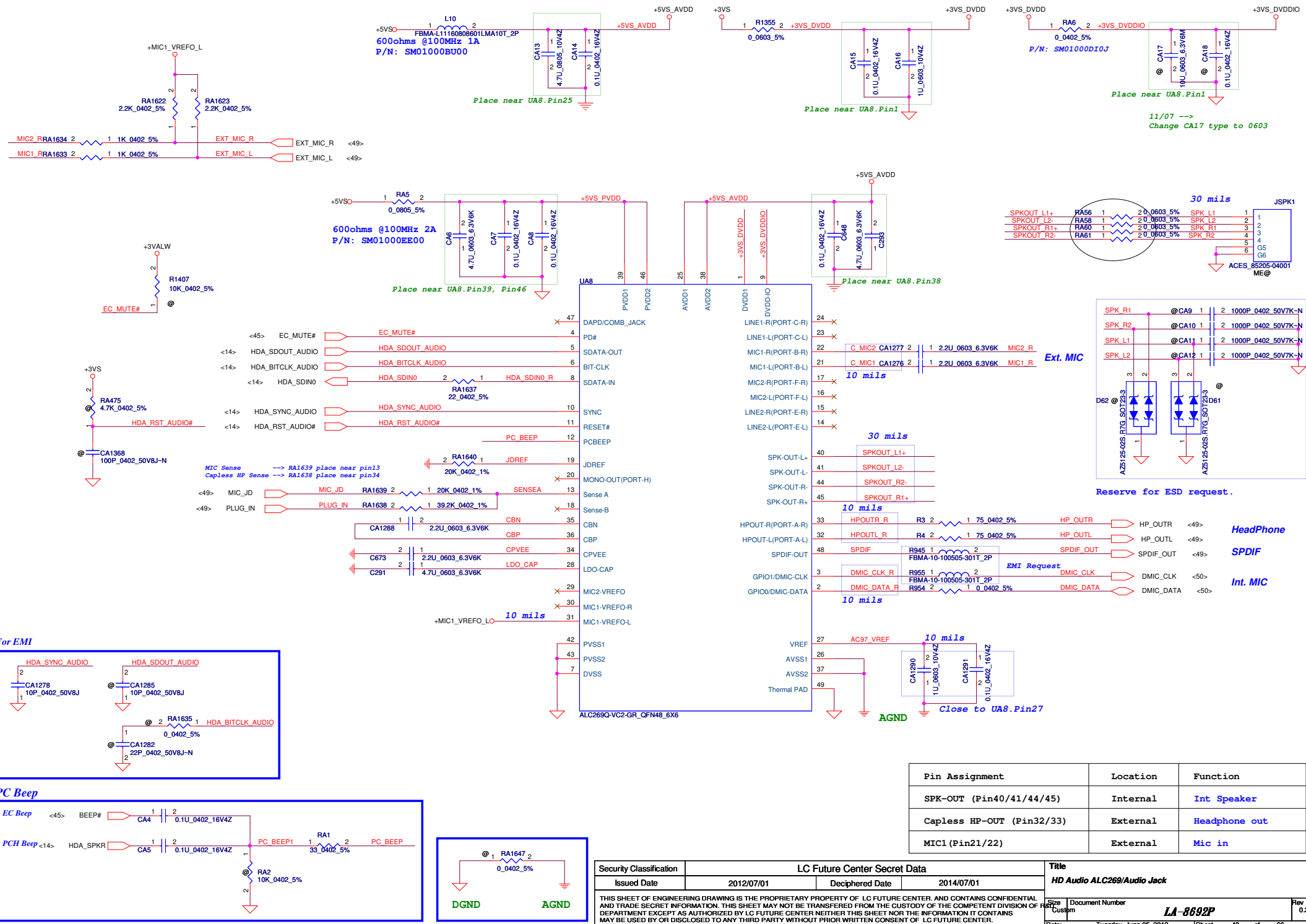
## SATA ODD Conn.



## ODD Power Control



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			Rev 0.2
			Date: Tuesday, June 05, 2012
			Sheet 42 of 66



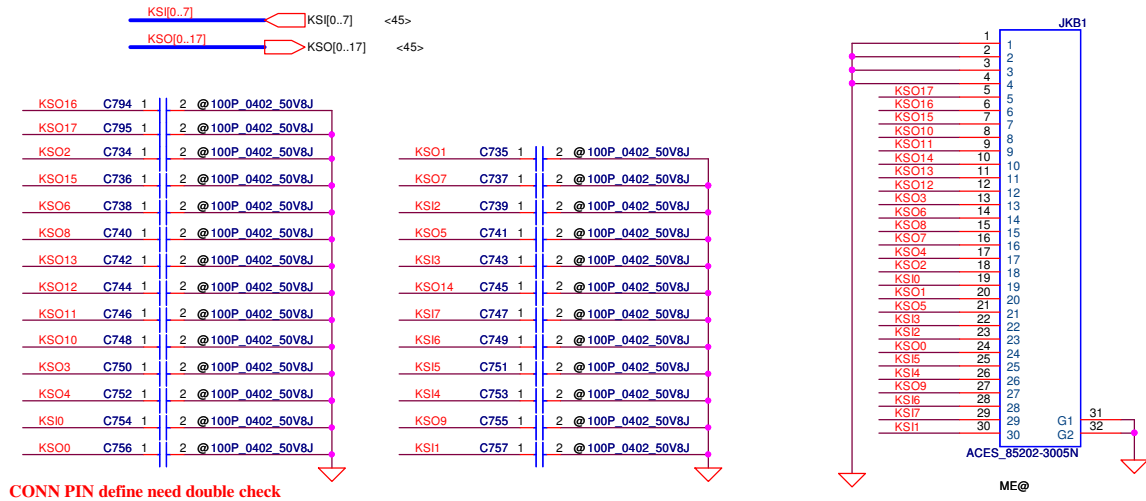
Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	HD Audio ALC269/Audio Jack	
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				Custom	0.1
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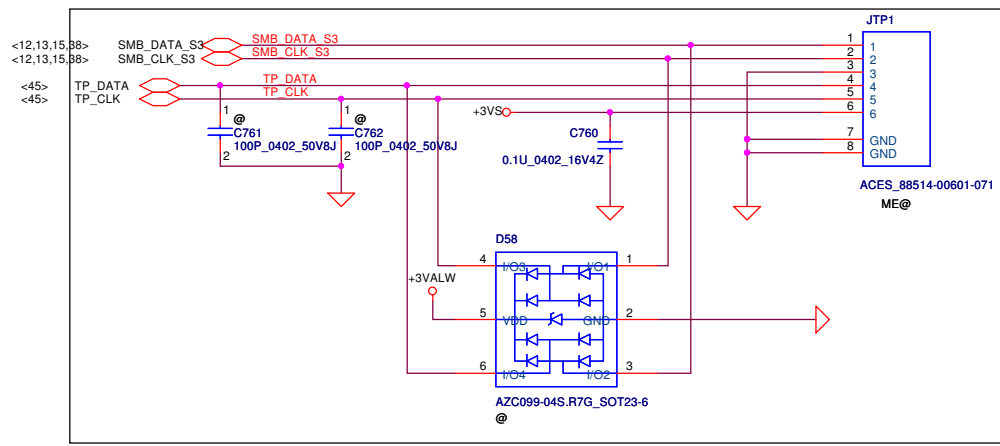




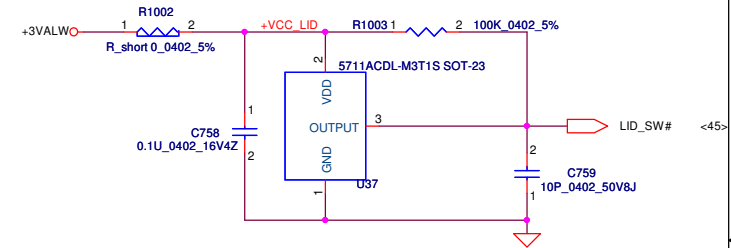
15" INT\_KBD Conn.

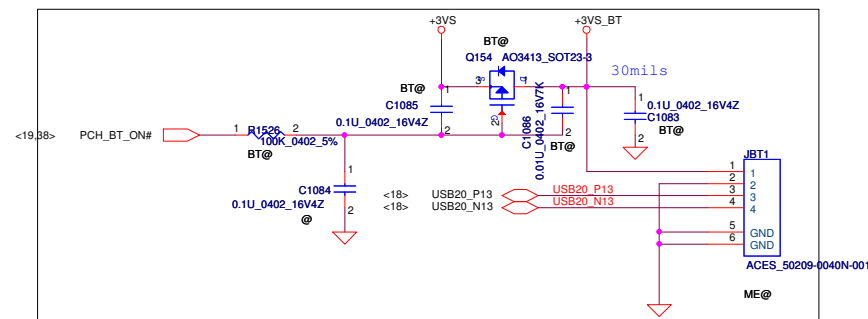
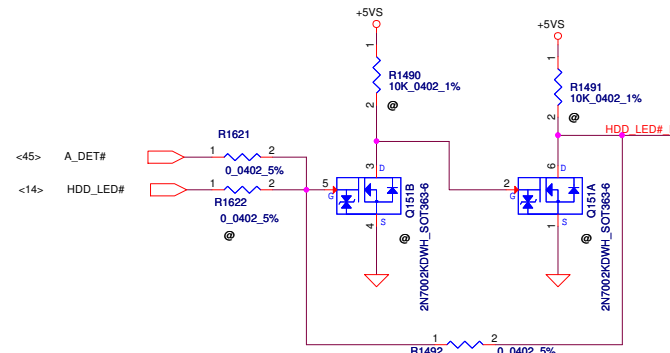
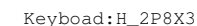
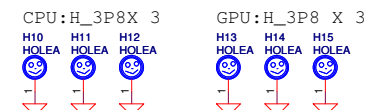
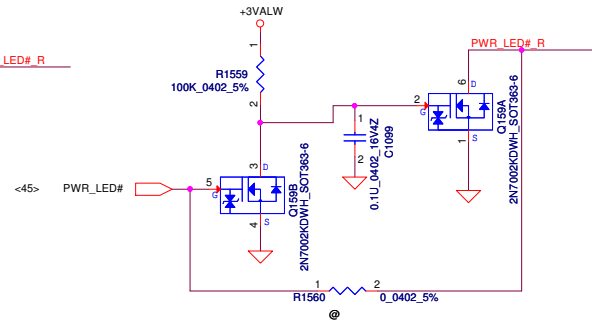


To TP/B Conn.



Lid Switch

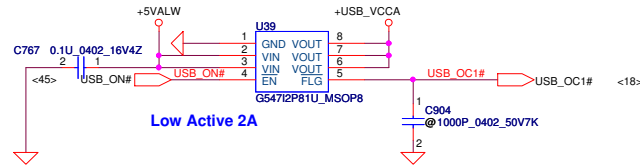




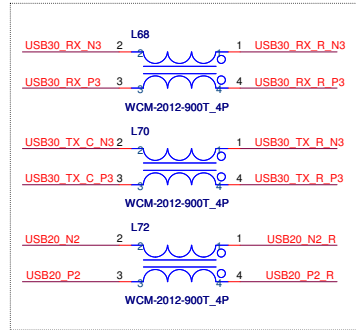
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	LED/EC SPI ROM/BT	
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Date:	Tuesday, June 05, 2012	Sheet	47	of	66



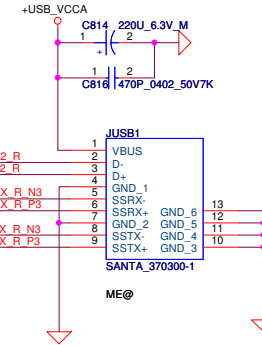
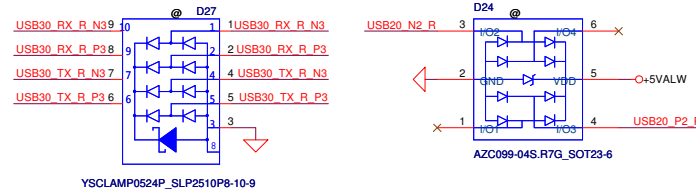
## LEFT SIDE USB3.0 PORT X1



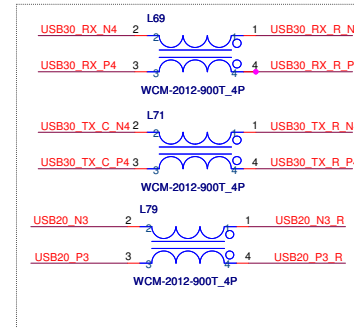
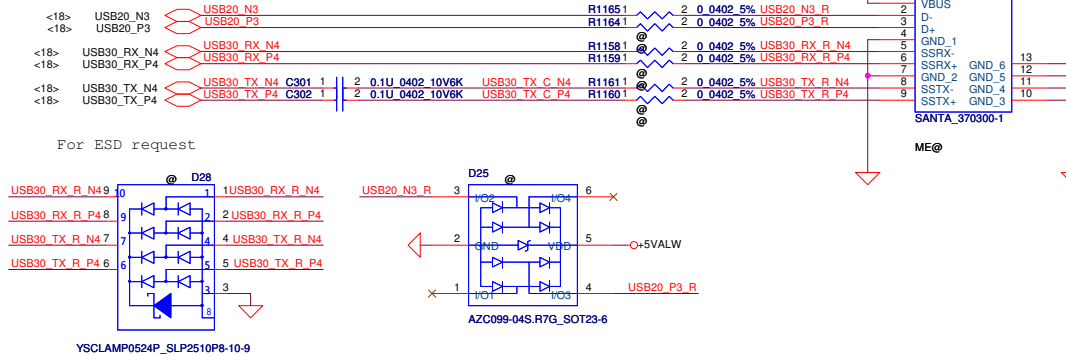
For EMI request  
 USB2.0 choke --> SM070000I00  
 USB3.0 Choke --> SM070001U00



For ESD request



For EMI request  
 USB2.0 choke --> SM070000I00  
 USB3.0 Choke --> SM070001U00

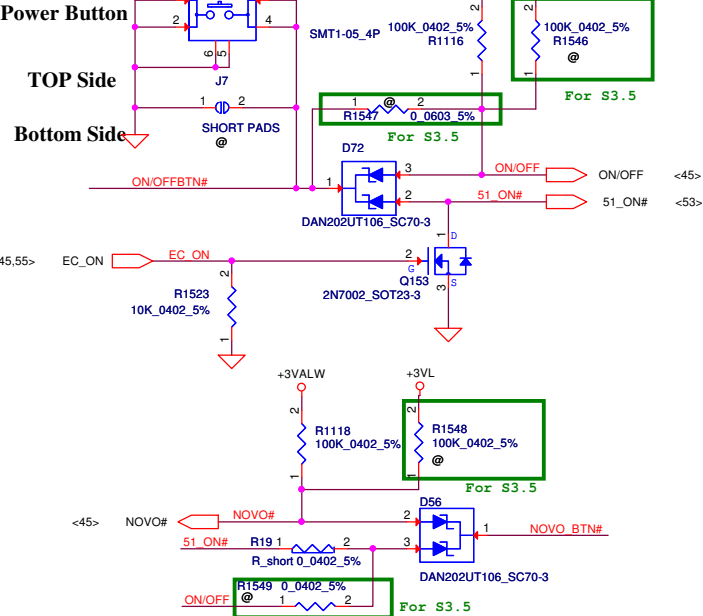


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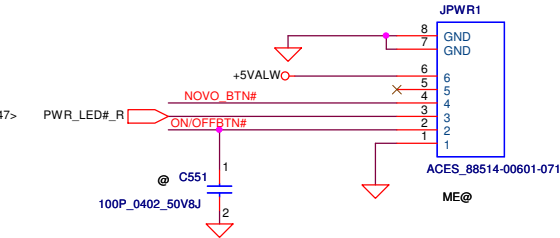




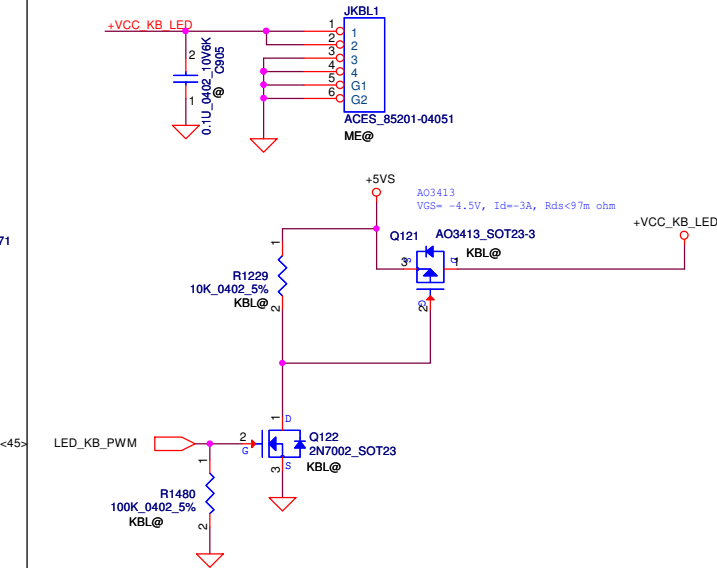
ON/OFF switch



Power Button/B link to Function/B Conn. 10pin



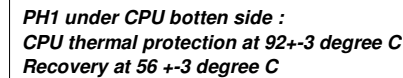
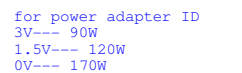
KB Lighting CONN.4pin



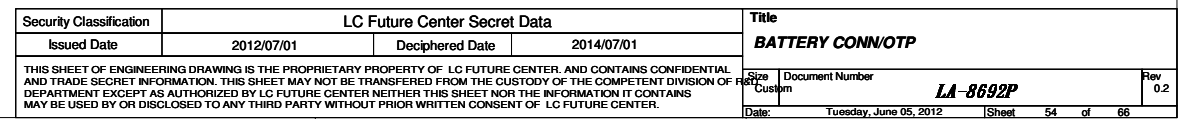
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	other IO connector	
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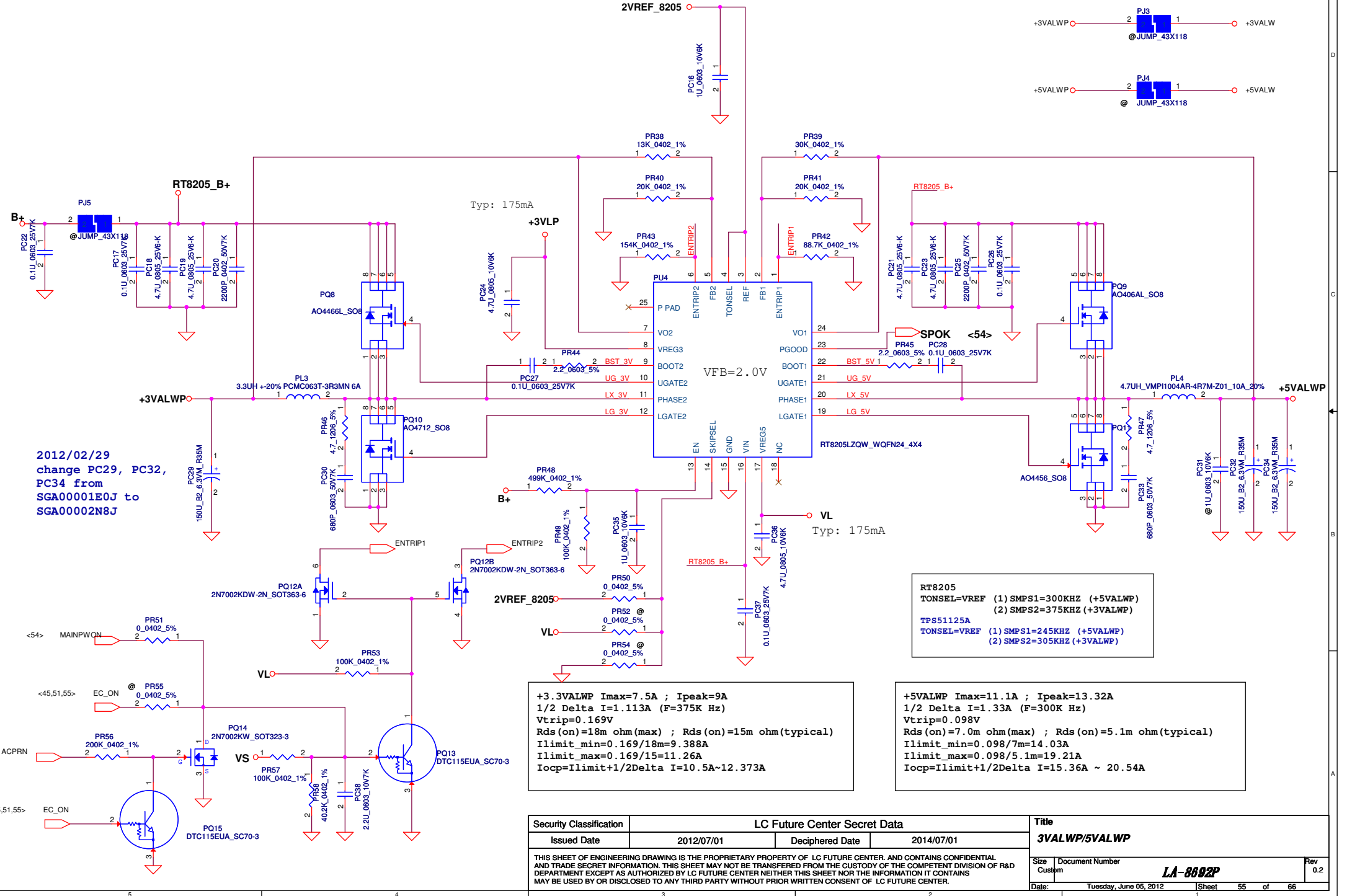


**For KB9012 (Red square) --> Remove PU1 circuit, but keep PR206  
PH201, PR205, PR211, PQ201, PR208, PR212**

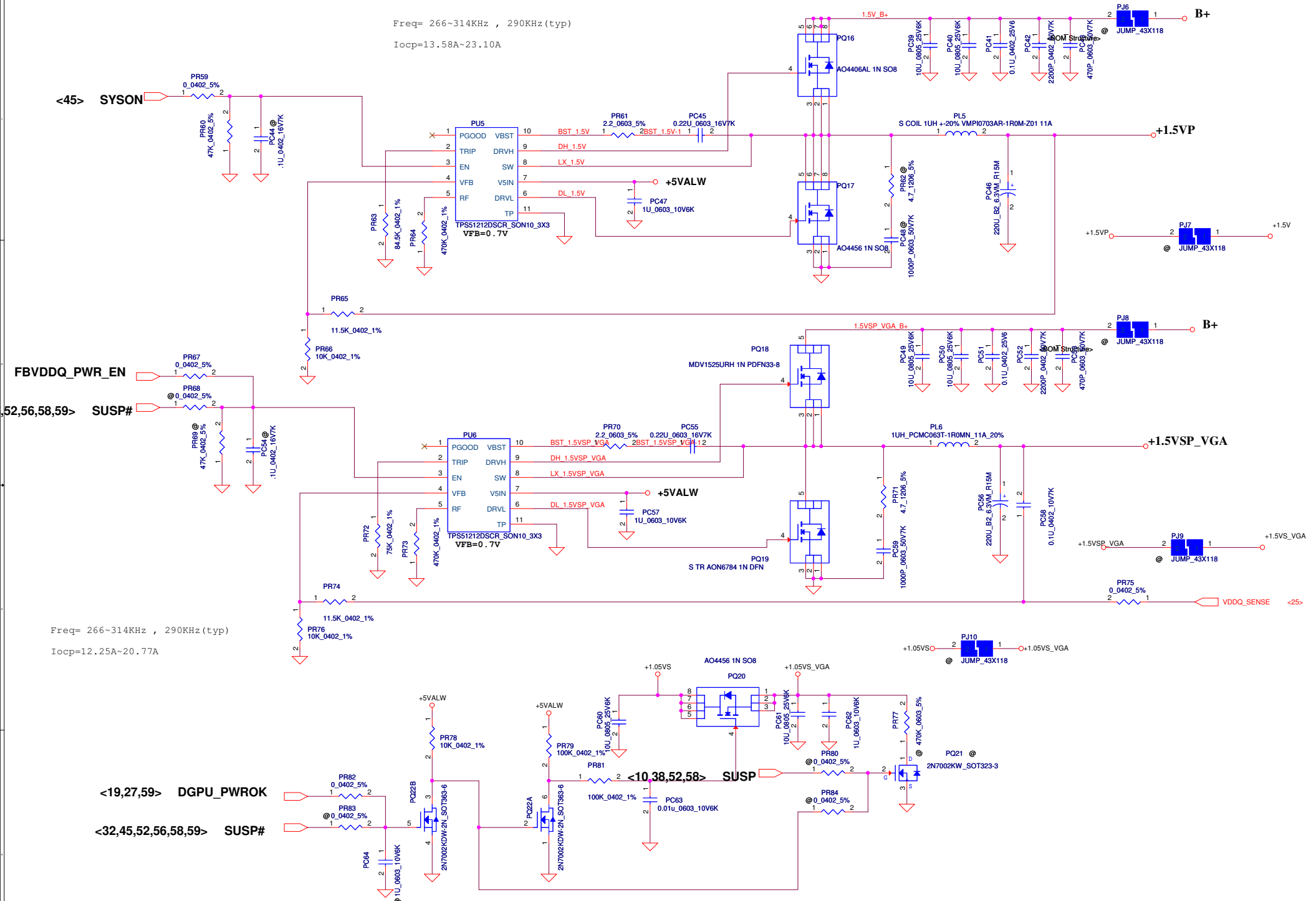




Note:  
Use TPS51125 IC can remove RTC refernece LDO  
Use TPS51427 IC must keep RTC refernece LDO



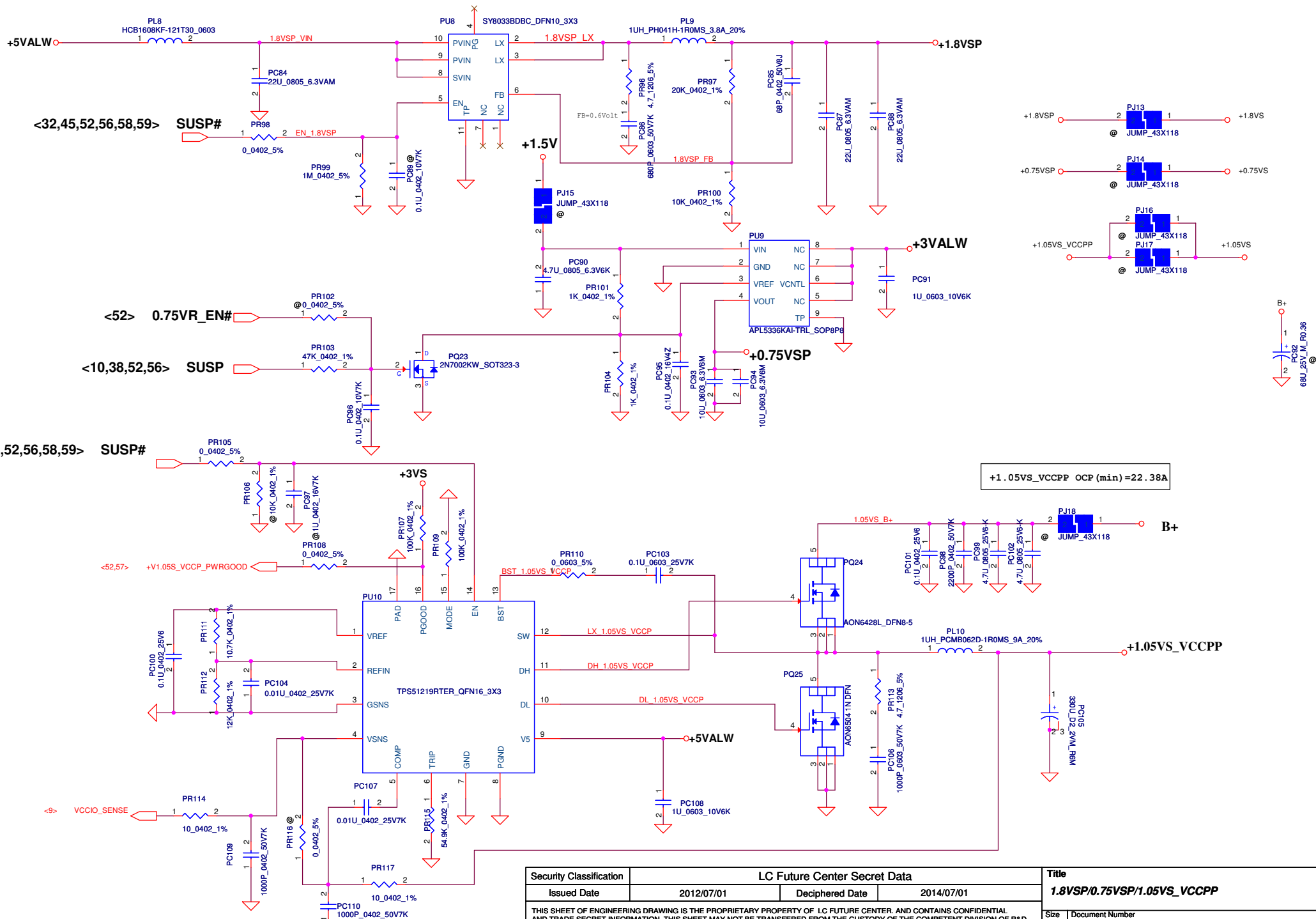
Freq= 266~314KHz , 290KHz(typ)  
Iocp=13.58A~23.10A



Freq= 266~314KHz , 290KHz(typ)  
Iocp=12.25A~20.77A

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GL1:0.9V(110000)  
GT:0.975V(101010)

2012/04/26  
change PC352 from @  
to Mount  
2012/04/26  
change PR313 from 0  
to 75K

PQ801@GL1  
PQ802@GL1

PQ806@GL1  
PQ808@GL1

Layout Note:  
Place near Phase1 Choke

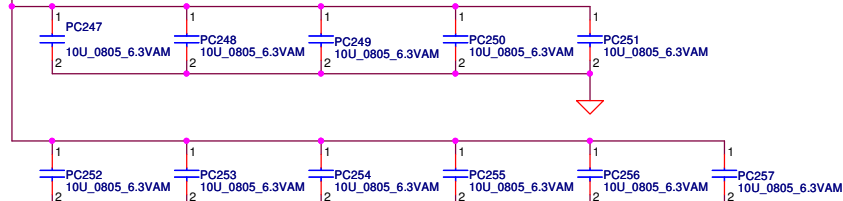
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2012/07/01	Deciphered Date	2014/07/01	VGA_COREP	
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				LA-8082P	
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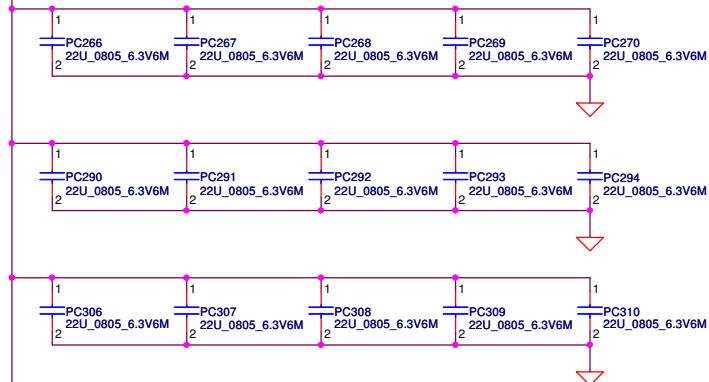




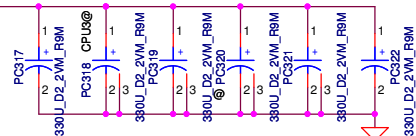
+VCC\_CORE



+VCC\_CORE



+VCC\_CORE



2012/02/29

DC:PC317, PC319, PC321, PC322 (330uF/9m +-20% \*4)

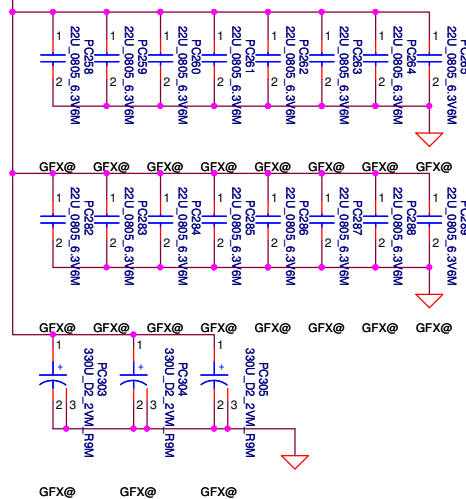
QC:PC317, PC318, PC319, PC321, PC322 (330uF/9m +-20% \*5)

P/N:SGA0000610J (no link)

+CPU\_CORE

+VCC\_GFXCORE\_AXG

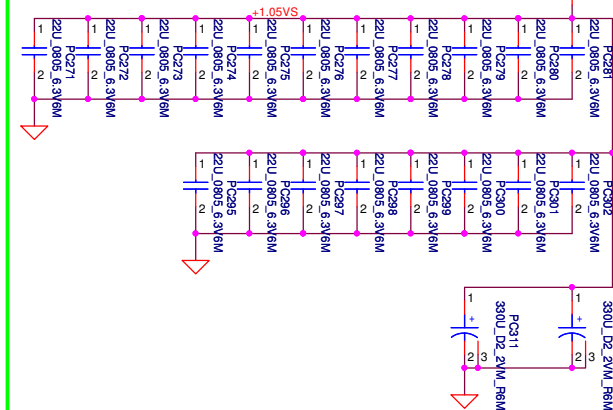
+VCC\_GFXCORE\_AXG



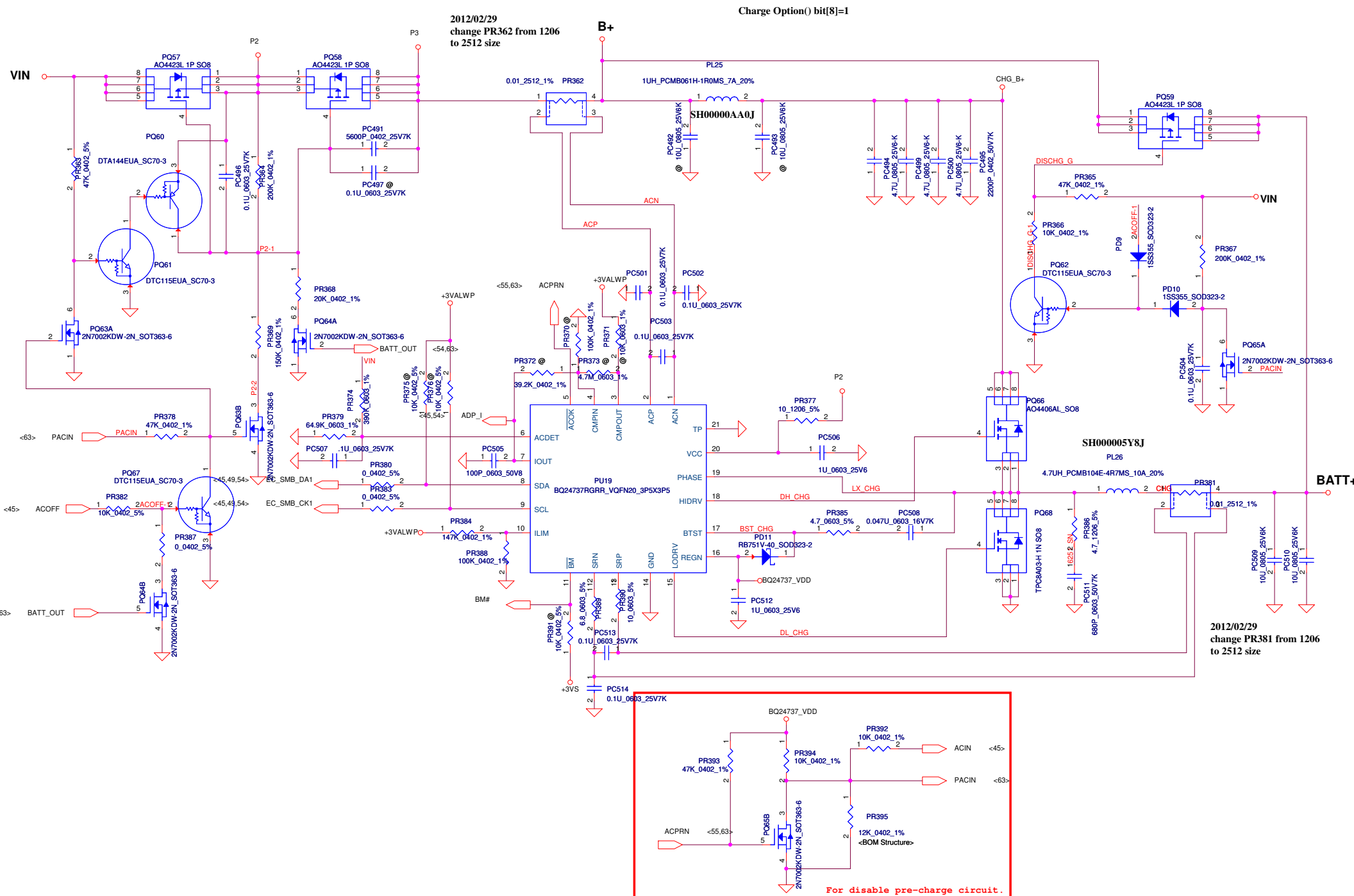
Below is 458544\_CRV\_PDDG\_0.5 Table 5-8.

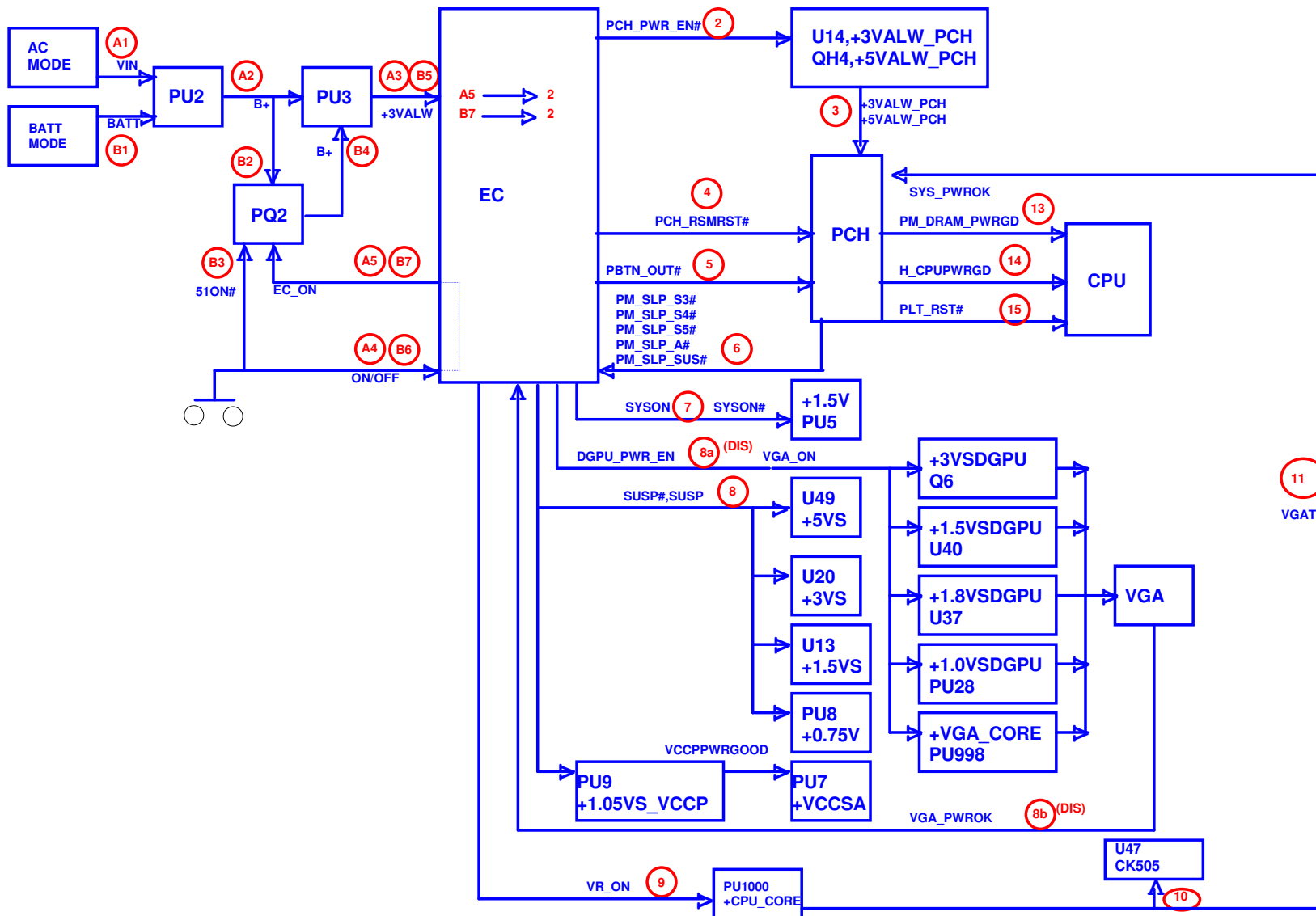
Socket Bottom	5 x 22 $\mu$ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 $\mu$ F (0805) 2 x (0805) no-stuff sites

+1.05VS



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## Version change list (P.I.R. List)

Page 1 of 1  
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Reserve 0.1uF for Charger IC	51	Reserve PC321	201109/27	B test
2	EMI Request		change PR322,PR407,PR408,PR503,PR511,PR606,PR804,PR827 to 2.2 ohm add PC526,PC527,PC970,PC971(470uF)	201109/27	B test
3	Combine 1.05V	51	Remove one power rail +V1.05S_VCCPP Pop PR722,PR712,PR718	201109/27	B test
4	Discharge for +1.05VS_VGA by NV Request	53	Reserve PR528	201109/27	B test
5	Set VGA_CORE VBOOT voltage	56	unpop PR806 change PR813 to 147K ohm	201109/27	B test
6	For VGA_CORE power saving by NV Request	56	add PR838 0ohm	201109/27	B test
7	for CPU_CORE load line adjust	57	add PC969	201109/27	B test
8	to prevent MOS over temperature	55/58	change PQ702,PQ901,PQ902,PQ905 TPCA8065	201109/27	B test
9	for CPU_CORE test	59	Reserve PC77,PC78	201109/27	B test
10	for VGA VID R-short	59	change PR318,PR319,PR320,PR321,PR322,PR323 footprint	201205/31	B test
11	Charger boost resistor For EMI	63	Change PR385 from 2.2ohm to 4.7ohm	201206/04	B test
12					
13					
14					
15					
16					
17					

Security Classification		LC Future Center Secret Data		Title	
Issued Date		2012/07/01		PIR (PWR)	
Deciphered Date		2014/07/01			
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QIWIY3 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
EVT TO DVT				
1		P7	Reserve R64	Reserve EC DRAMRST control pin for Deep S3
2		P16	Reserve R1457, R1455, R1447	Reserve SUSACK#, SUSWARN#, SLP_SUS# control signal for Deep S3
3		P16	Reserve Q118, R1120, R1121	Reverse SLP_SUS# to control +3V_PCH&+5V_PCH
4		P16	Change AC_PRESENT Pull high source to +3V_DSW	For Deep S3 function
5		P21	Remove R289	+5V_PCH control circuit change for Deep S3
6		P36	Reserve J8, Q104, C533, C526, R436	Reserve for AOAC function
7		P36	Change JP1 pin2, 24, 52 power source to +3VS_WLAN_AOAC	Reserve for AOAC function
8		P42	Change EC GPIO pin setting (Impact pin 18, 71, 72, 126, 128)	For DeepS3/AOAC function
9		P48	Reserve J11, J14, Q148, Q149, C38, C39	+3V_PCH&+5V_PCH control circuit for Deep S3
10		P45	change U49 symbol (without GND pad)	For Dfx issue
11		P46	change U40, U69 symbol (without GND pad)	For Dfx issue
12		P47	change JP10 type to SP01001B800	For Dfx issue
13		P19	Reserve R207, R224 to contact WLAN wake even	Reserve for AOAC function
14		P41	Change JSPK1 type to SP02000H700	For Dfx issue
14		P19	Reserve R704 and R706 for GPIO69 PU&PD	For SKU ID
15		P23	Change CV37, CV38 to 22P	For Crystal EA request
16		P37	Change C968, C969 to 33P	For Crystal EA request